Intel® E7210 Memory Controller Hub (MCH) Chipset

Datasheet

Revision 1.0

February 2004

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Contents

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Revision History

Revision	Description	Date
-001	• Initial Release	February 2004

Canterwood-ES MCH Chipset Features

- Host Interface Support:
  - Intel® Pentium® 4 processor with 512-KB L2 Cache on 0.13 micron process / processor code named Prescott
  - VTT 1.1 V – 1.55 V ranges
  - 64-bit FSB frequencies of 400 MHz (100 MHz bus clock), 533 MHz (133 MHz bus clock), and 800 MHz (200 MHz bus clock). Maximum theoretical BW of 6.4 GB/s.
  - FSB Dynamic Bus Inversion on the data bus
  - 32-bit addressing for access to 4 GB of memory space
  - 12-deep In Order Queue
  - AGTL+ On-die Termination (ODT)
  - Hyper-Threading Technology
- System Memory Controller (DDR) Support:
  - Dual-channel (128 bits wide for non-ECC or 144 bits wide for ECC) DDR memory interface
  - Single-channel (64 bits wide for non-ECC or 72 bits wide for ECC) DDR memory interface
  - Symmetric and asymmetric memory dual-channel upgrade
  - 128-Mb, 256-Mb, 512-Mb technologies implemented as x8, x16 devices
  - four bank devices
  - Non-ECC and ECC, un-buffered DIMMS only
  - Maximum of two DIMMs per channel, with each DIMM having one or two rows
  - Up to 4 GB system memory
  - Up to 16 simultaneously-open pages (four per row) in dual-channel mode and up to 32 open pages in single-channel mode
  - 4-KB to 64-KB page sizes (4 KB to 32 KB in single-channel, 8 KB to 64 KB in dual-channel)
  - Opportunistic refresh
  - Suspend-to-RAM support using CKE(S3)
  - SPD (Serial Presence Detect) Scheme for DIMM Detection
  - DDR (Double Data Rate type 1):
    - Maximum of two DDR DIMMs per channel, single-sided and/or double-sided
    - DDR266, DDR333, DDR400 DIMM modules
    - DDR channel operation at 266 MHz, 333 MHz and 400 MHz with a Peak BW of 2.1 GB/s, 2.7 GB/s, and 3.2 GB/s respectively per channel
    - Burst length of 4 and 8 for single-channel (32 or 64 bytes per access, respectively); for dual-channel a burst of 4 (64 bytes per access)
    - SSTL_2 signaling
- Communication Streaming Architecture (CSA) Interface Support:
  - 8-bit Hub Interface 1.5 electrical/transfer protocols.
  - 266 MB/s point-to-point connection to MCH
  - Gigabit Ethernet (GbE) supported
  - 1.5 V operation
- Hub Interface (HI) Support:
  - Hub Interface 1.5
  - 266 MB/s point-to-point Hub Interface to the ICH
  - 66 MHz base clock
  - 1.5 V operation
- MCH Package:
  - 42.5 mm x 42.5 mm Flip Chip Ball Grid Array (FC-BGA) package
  - 1005 solder balls

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Introduction 1

The Intel® E7210 chipset is designed for systems based on the Intel® Pentium® 4 processor with 512-KB L2 cache on 0.13 micron process in the 478-pin package or the processor code named Prescott and supports front-side bus (FSB) frequencies of 400 MHz, 533 MHz, and 800 MHz. The Intel E7210 chipset contains two main components: Memory Controller Hub (MCH) for the host bridge and I/O Controller Hub for the I/O subsystem. The Intel E7210 chipset uses the Intel® 6300ESB I/O Controller Hub (ICH) for the I/O Controller Hub. This document is the datasheet for the Intel E7210 MCH component.

The Intel E7210 chipset platform supports the following processors:

- Pentium 4 processor with 512-KB L2 cache on 0.13 micron process in the 478-pin package.
- Processor code named Prescott. The processor code named Prescott returns a processor signature of 00000F3xh when the CPUID instruction is executed with EAX=1.

Note: Unless otherwise specified, the term ICH in this document refers to the Intel 6300ESB I/O Controller Hub.

Note: Unless otherwise specified, the term processor in this document refers to the Pentium 4 processor with 512-KB L2 cache on 0.13 micron process in the 478-pin package and processor code named Prescott.

1.1 Terminology

This section provides the definitions of some of the terms used in this document.

Table 1. General Terminology

Terminology	Description
Bank	DRAM chips are divided into multiple banks internally. Commodity parts are all 4 bank, which is the only type the MCH supports. Each bank acts somewhat like a separate DRAM, opening and closing pages independently, allowing different pages to be open in each. Most commands to a DRAM target a specific bank, but some commands (i.e., Precharge All) are targeted at all banks. Multiple banks allows higher performance by interleaving the banks and reducing page miss cycles.
Channel	In the MCH a DRAM channel is the set of signals that connects to one set of DRAM DIMMs. The MCH has two DRAM channels, (a pair of DIMMs added at a time, one on each channel).
Chipset Core	The MCH internal base logic.
Column Address	The column address selects one DRAM location, or the starting location of a burst, from within the open page on a read or write command.
Double-Sided DIMM	Terminology often used to describe a DIMM that contain two DRAM rows. Generally a Double-sided DIMM contains two rows, with the exception noted above. This terminology is not used within this document.
DDR	Double Data Rate SDRAM. DDR describes the type of DRAMs that transfers two data items per clock on each pin. This is the only type of DRAM supported by the MCH.
ECC	ERROR Checking and Correction. ECC describes a DRAM feature to detect bit errors.
Full Reset	A Full MCH Reset is defined in this document when RSTIN# is asserted.

Table 1. General Terminology (Continued)

Terminology	Description
MCH	The Memory Controller Hub component that contains the processor interface, DRAM controller, CSA interface, and AGP interface. It communicates with the I/O controller hub (ICH) over a proprietary interconnect called the hub interface (HI).
HI	Hub Interface. HI is the proprietary hub interconnect that connects the MCH to the ICH. In this document HI cycles originating from or destined for the primary PCI interface on the ICH are generally referred to as HI/PCI or simply HI cycles.
Host	This term is used synonymously with processor.
ICH	Intel® 6300ESB I/O Controller Hub component.
Primary PCI	The physical PCI bus that is driven directly by the ICH component. Communication between PCI and the MCH occurs over HI. Note that even though the Primary PCI bus is referred to as PCI it is **not** PCI Bus 0 from a configuration standpoint.
FSB	Processor Front-Side Bus. This is the bus that connects the processor to the MCH.
Row	A group of DRAM chips that fill out the data bus width of the system and are accessed in parallel by each DRAM command.
Row Address	The row address is presented to the DRAMs during an Activate command, and indicates which page to open within the specified bank (the bank number is presented also).
Scalable Bus	Processor-to-MCH interface. The compatible mode of the Scalable Bus is the P6 Bus. The enhanced mode of the Scalable Bus is the P6 Bus plus enhancements primarily consisting of source synchronous transfers for address and data, and FSB interrupt delivery. The Intel® Pentium® 4 processor implements a subset of the enhanced mode.
Single-Sided DIMM	Terminology often used to describe a DIMM that contains one DRAM row. Usually one row fits on a single side of the DIMM allowing the backside to be empty.
SDR	Single Data Rate SDRAM.
SDRAM	Synchronous Dynamic Random Access Memory.
Secondary PCI	The physical PCI interface that is a subset of the AGP bus driven directly by the MCH. It supports a subset of 32-bit, 66 MHz PCI 2.0 compliant components, but only at 1.5 V (not 3.3 V or 5 V).
SSTL_2	Stub Series Terminated Logic for 2.6 Volts (DDR)

1.2 Related Documents

Document	Document Number/ Location
Intel® E7210 Chipset: For use with Intel® Pentium®4 Processors with 512-KB L2 Cache on 0.13 Micron Process Platform Design Guide	http://developer.intel.com/design/chipsets/designex/252527.htm
Intel® E7210 Chipset: Intel® E7210 MCH Thermal Design Guide	http://developer.intel.com/design/chipsets/designex/252528.htm
Intel® 6300ESB I/O Controller Hub (ICH) EDS	Available on IBL
Intel ® Pentium ® 4 Processor with 512-KB L2 Cache on 0.13 Micron Process Datasheet: 2 GHz – 3.06 GHz Frequencies Supporting Hyper-Threading Technology(1) at 3.06 GHz with 533 MHz System Bus and All Frequencies with 800 MHz System Bus	http://developer.intel.com/design/pentium4/datashts/298643.htm
JEDEC Double Data Rate (DDR) SDRAM Specification	www.jedec.org
PC SDRAM Specification	http://developer.intel.com/technology/memory/pcsdram/spec/index.htm

NOTE: For additional related documents, refer to the *Intel® E7210 Chipset: For use with Intel® Pentium® 4 Processors with 512-KB L2 Cache on 0.13 Micron Process Platform Design Guide*.

1.3 Intel® E7210 Chipset System Overview

Note: Figure 1 shows an example block diagram of an Intel E7210 chipset-based platform. The Intel E7210 chipset is designed for use in a desktop system based on the Pentium 4 processor with 512-KB L2 cache on 0.13 micron process in a 478-pin package and the processor code named Prescott. The processor interface supports the Pentium 4 processor subset of the Extended Mode of the Scalable Bus Protocol. In a Intel E7210 chipset-based platform, the MCH provides the processor interface, system memory interface, CSA interface and hub interface.

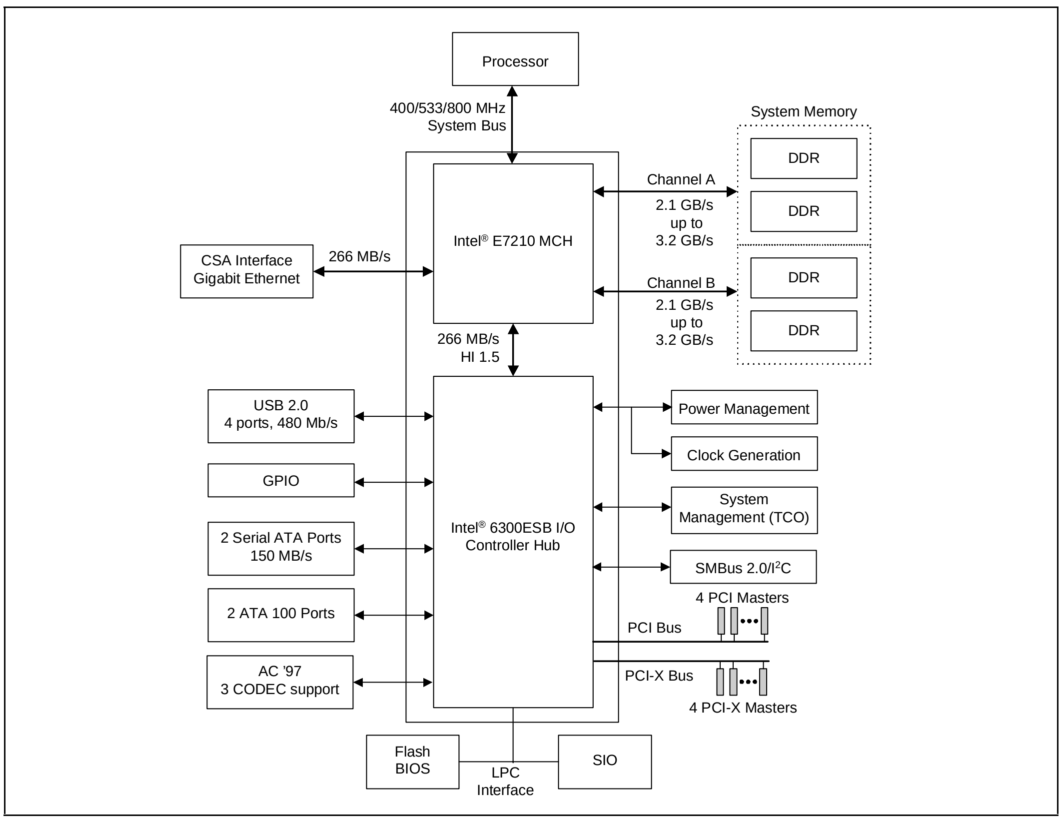
The MCH provides a Communications Streaming Architecture (CSA) Interface that connects the MCH to a Gigabit Ethernet (GbE) controller.

The Intel E7210 chipset platform support 4 GB of system memory. The memory can be 266/333/400 MHz Double Data Rate (DDR) memory components with a 64-bit wide data bus. Available bandwidth is 6.4 GB/s using DDR400 in dual-channel mode.

The Intel 6300ESB I/O Controller Hub integrates an Ultra ATA 100 controller, two Serial ATA host controllers, one EHCI host controller, two UHCI host controllers supporting four external USB 2.0 ports, LPC interface controller, flash BIOS interface controller, PCI-X interface controller, PCI interface controller, AC ‘97 digital controller and a hub interface for communication with the MCH. The Intel 6300ESB I/O Controller Hub component provides the data buffering and interface arbitration required to ensure that system interfaces operate efficiently and provide the bandwidth necessary to enable the system to obtain peak performance.

The ACPI compliant Intel 6300ESB I/O Controller Hub platform can support the Full-on, Stop Grant, Suspend to RAM, Suspend to Disk, and Soft-Off power management states.

Figure 1. Intel® E7210/Intel® 6300ESB ICH Chipset System Block Diagram



1.4 Intel® E7210 MCH Overview

The Intel E7210 MCH provides the host bridge interfaces in a Intel E7210 chipset based platform. The MCH contains advanced desktop power management logic.

The MCH's role in a system is to manage the flow of information between its four interfaces: the processor front-side bus (FSB), the memory attached to the DRAM controller, the Hub Interface, and CSA interface. This includes arbitrating between the four interfaces when each initiates an operation. To increase system performance, the MCH incorporates several queues and a write cache.

The MCH supports Performance Acceleration Technology (PAT). PAT is only available when the MCH is set at FSB 800 MHz and DDR 400 MHz mode. PAT enables lower latency paths from the FSB to system memory. This enables increased system performance for the Intel E7210 chipset system.

1.4.1 Host Interface

The Intel E7210 MCH is designed for use with a single UP processor in a 478-pin package. The processor interface supports the Pentium 4 processor subset of the extended mode of the Scalable Bus Protocol. The MCH supports FSB frequencies of 400 MHz, 533 MHz, and 800 MHz (100 MHz, 133 MHz, and 200 MHz HCLK, respectively) using a scalable FSB VCC_CPU. The MCH supports 32-bit host addressing, decoding up to 4 GB of the processor's memory address space.

Host-initiated I/O cycles are decoded to hub interface, or MCH configuration space. Host-initiated memory cycles are decoded to hub interface, or system memory. Memory accesses initiated from the hub interface to system memory are snooped on the host bus.

1.4.2 System Memory Interface

The MCH integrates a system memory DDR controller with two 64-bit wide interfaces. Only Double Data Rate (DDR) memory is supported; consequently, the buffers support only SSTL_2 signal interfaces. The memory controller interface is fully configurable through a set of control registers.

System Memory Interface

- Supports one or two, 64-bit wide DDR data channels with 1 or 2 DIMMs per-channel.
- Available bandwidth up to 3.2 GB/s (DDR400) for single-channel mode and 6.4 GB/s (DDR400) in dual-channel mode.
- Configurable optional ECC operation (single-bit Error Correction and multiple-bit Error Detection).
- Supports 128-Mb, 256-Mb, 512-Mb DDR technologies.
- Supports only x8, x16, DDR devices with four banks.
- Does not support double sided x16 DIMMS.
- Registered DIMMs not supported.
- Supports opportunistic refresh.
- SPD (Serial Presence Detect) scheme for DIMM detection support.
- Suspend-to-RAM support using CKE.

- Supports configurations defined in the JEDEC DDR1 DIMM specification only.
- Performance Acceleration Technology support.

Single-Channel DDR Configuration

- Up to 4.0 GB of DDR.
- Supports up to four DDR DIMMs (two DIMMs per channel), single-sided and/or double-sided.
- Supports DDR266, DDR333, or DDR400 unregistered ECC or non-ECC DDR DIMMs.
- Supports up to 32 simultaneously open pages.
- Does not support mixed-mode / uneven double-sided DDR DIMMs.

Dual-Channel DDR Configuration - Lockstep

- Up to 4.0 GB of DDR.
- Supports up to four DDR DIMMs (two DIMMs per channel), single-sided and/or double-sided.
- DIMMS must be populated in identical pairs for dual-channel operation.
- Supports 16 simultaneously open pages (four per row).
- Supports DDR266, DDR333, or DDR400 unregistered non-ECC or ECC DDR DIMMs.

1.4.3 Hub Interface

The Hub Interface (HI) connects the MCH to the I/O Controller Hub (ICH). Most communication between the MCH and the ICH occurs over the hub interface. The MCH supports HI 1.5 that uses HI 1.0 protocol with HI 2.0 electrical characteristics. The hub interface runs at 266 MT/s (with 66-MHz base clock) and uses 1.5 V signaling.

1.4.4 Communications Streaming Architecture (CSA) Interface

The CSA interface connects the MCH with a Gigabit Ethernet (GbE) controller. The MCH supports HI 1.5 over the interface that uses a HI 1.0 protocol with HI 2.0 electrical characteristics. The CSA interface runs at 266 MT/s (with 66-MHz base clock) and uses 1.5 V signaling.

1.5 Clock Ratios

Table 2 lists the supported system memory clock ratios. CSA, and HI run at 66-MHz common clock and are asynchronous to the chipset core. There is no required skew or ratio between FSB/ chipset core and 66-MHz system clocks.

Table 2. System Memory Clock Ratios

FSB	Host Clock	DRAM Clock	Ratios	DRAM Data Rate	DRAM Type	Peak Bandwidth
400 MHz	100 MHz	133 MHz	3/4	266 MT/s	DDR-DRAM	2.1 GB/s
533 MHz	133 MHz	133 MHz	1/1	266 MT/s	DDR-DRAM	2.1 GB/s
800 MHz	200 MHz	133 MHz	3/2	266 MT/s	DDR-DRAM	2.1 GB/s

Table 2. System Memory Clock Ratios (Continued)

FSB	Host Clock	DRAM Clock	Ratios	DRAM Data Rate	DRAM Type	Peak Bandwidth
533 MHz	133 MHz	166 MHz	4/5	333 MT/s	DDR-DRAM	2.7 GB/s
800 MHz	200 MHz	160 MHz	5/4	320 MT/s	DDR-DRAM	2.6 GB/s
800 MHz	200 MHz	200 MHz	1/1	400 MT/s	DDR-DRAM	3.2 GB/s

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Signal Description 2

This section provides a detailed description of MCH signals. The signals are arranged in functional groups according to their associated interface.

The “#” symbol at the end of a signal name indicates that the active, or asserted state occurs when the signal is at a low voltage level. When “#” is not present after the signal name the signal is asserted when at the high voltage level.

The following notations are used to describe the signal type:

I	Input pin
O	Output pin
I/O	Bi-directional Input/Output pin
s/t/s	Sustained Tri-state. This pin is driven to its inactive state prior to tri-stating.

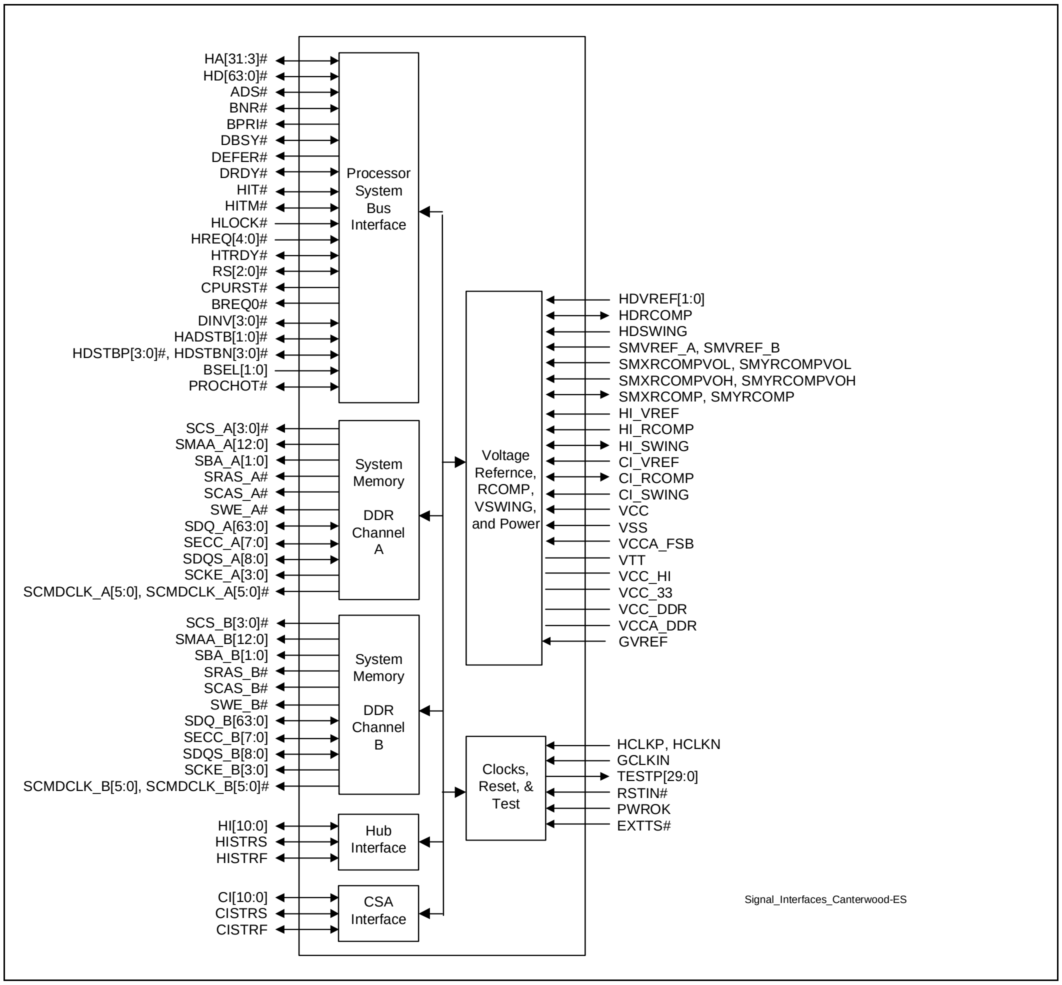
The signal description also includes the type of buffer used for the particular signal:

AGP	AGP interface signals. These signals are compatible with AGP 2.0 1.5 V signaling and AGP 3.0 0.8 V swing signaling environment DC and AC specifications. The buffers are not 3.3 V tolerant.
AGTL+	Open Drain AGTL+ interface signal. Refer to the AGTL+ I/O Specification for complete details. The MCH integrates AGTL+ termination resistors, and supports VTT from 1.15 V to 1.55 V.
HI15	Hub Interface 1.5 compatible signals and CSA signals
LVTTL	Low Voltage TTL 3.3 V compatible signals
SSTL_2	Stub Series Terminated Logic 2.6 V compatible signals
2.6 VGPIO	2.6 V buffers used for miscellaneous GPIO signals
CMOS	CMOS buffers

Host Interface signals that perform multiple transfers per clock cycle may be marked as either “4x” (for signals that are “quad-pumped”) or 2x (for signals that are “double-pumped”).

Note: Processor address and data bus signals are logically inverted signals. In other words, the actual values are inverted of what appears on the processor bus. This must be taken into account and the addresses and data bus signals must be inverted inside the MCH host bridge. All processor control signals follow normal convention. A 0 indicates an active level (low voltage) if the signal is followed by # symbol and a 1 indicates an active level (high voltage) if the signal has no # suffix.

Figure 2. Intel® E7210 MCH Interface Block Diagram



2.1 Host Interface Signals

Signal Name	Type	Description
ADS#	I/O AGTL+	**Address Strobe**: The processor bus owner asserts ADS# to indicate the first of two cycles of a request phase. The MCH can assert this signal for snoop cycles and interrupt messages.
BNR#	I/O AGTL+	**Block Next Request**: This signal is used to block the current request bus owner from issuing a new request. This signal is used to dynamically control the processor bus pipeline depth.
BPRI#	O AGTL+	**Priority Agent Bus Request**: The MCH is the only Priority Agent on the processor bus. It asserts this signal to obtain ownership of the address bus. This signal has priority over symmetric bus requests and cause the current symmetric owner to stop issuing new transactions unless the HLOCK# signal was asserted.
BREQ0#	O AGTL+	**Bus Request 0#**: The MCH pulls the BREQ0# signal low during CPURST#. The signal is sampled by the processor on the active-to-inactive transition of CPURST#. The minimum setup time for this signal is 4 HCLKs. The minimum hold time is 2 clocks and the maximum hold time is 20 HCLKs. BREQ0# should be terminated high (Pulled up) after the hold time requirement has been satisfied. **NOTE:** This signal is called BR0# in the Intel processor specification.

Signal Name	Type	Description
BSEL[1:0]	I CMOS	**Core / FSB Frequency**: (FSBFREQ) Select Strap. This strap is latched at the rising edge of PWROK. These pins have no default internal pull-up resistor. 00 = Core frequency is 100 MHz, FSB frequency is 400 MHz 01 = Core frequency is 133 MHz, FSB frequency is 533 MHz 10 = Core Frequency is 200 MHz, FSB frequency is 800 MHz 11 = Reserved
CPURST#	O AGTL+	**CPU Reset**: The CPURST# pin is an output from the MCH. The MCH asserts CPURST# while RSTIN# (PCIRST# from ICH) is asserted and for approximately 1 ms after RSTIN# is deasserted. The CPURST# allows the processors to begin execution in a known state. Note that the ICH must provide processor frequency select strap setup and hold times around CPURST#. This requires strict synchronization between MCH CPURST# deassertion and ICH driving the straps.
DBSY#	I/O AGTL+	**Data Bus Busy**: This signal is used by the data bus owner to hold the data bus for transfers requiring more than one cycle.
DEFER#	O AGTL+	**Defer**: DEFER# indicates that the MCH will terminate the transaction currently being snooped with either a deferred response or with a retry response.
DINV[3:0]#	I/O AGTL+ 4X	**Dynamic Bus Inversion**: These signals are driven along with the HD[63:0]# signals. They indicate if the associated signals are inverted. DINV[3:0]# are asserted such that the number of data bits driven electrically low (low voltage) within the corresponding 16-bit group never exceeds 8. **DINV[x]#** **Data Bits** DINV3# HD[63:48]# DINV2# HD[47:32]# DINV1# HD[31:16]# DINV0# HD[15:0]# **NOTE:** This signal is called DBI[3:0] in the Intel processor specification.
DRDY#	I/O AGTL+	**Data Ready:** This signal is asserted for each cycle that data is transferred.
HA[31:3]#	I/O AGTL+ 2X	**Host Address Bus:** HA[31:3]# connect to the processor address bus. During processor cycles, HA[31:3]# are inputs. The MCH drives HA[31:3]# during snoop cycles on behalf of HI and Secondary PCI initiators. HA[31:3]# are transferred at 2X rate. Note that the address is inverted on the processor bus. **NOTE:** The MCH drives the HA7# signal, which is then sampled by the processor and the MCH on the active-to-inactive transition of CPURST#. The minimum setup time for this signal is 4 HCLKs. The minimum hold time is 2 clocks and the maximum hold time is 20 HCLKs.
HADSTB[1:0]#	I/O AGTL+ 2X	**Host Address Strobe:** HADSTB[1:0]# are source synchronous strobes used to transfer HA[31:3]# and HREQ[4:0]# at the 2X transfer rate. **Strobe** **Address Bits** HADSTB0# A[16:3]#, REQ[4:0]# HADSTB1# A[31:17]#
HD[63:0]#	I/O AGTL+ 4X	**Host Data:** These signals are connected to the processor data bus. Data on HD[63:0]# is transferred at a 4X rate. Note that the data signals may be inverted on the processor bus, depending on the DINV[3:0] signals.
HDSTBP[3:0]# HDSTBN[3:0]#	I/O AGTL+ 4X	**Differential Host Data Strobes**: The differential source synchronous strobes used to transfer HD[63:0]# and DINV[3:0]# at the 4X transfer rate. **Strobe** **Data Bits** HDSTBP3#, HDSTBN3# HD[63:48]#, DINV3# HDSTBP2#, HDSTBN2# HD[47:32]#, DINV2# HDSTBP1#, HDSTBN1# HD[31:16]#, DINV1# HDSTBP0#, HDSTBN0# HD[15:0]#, DINV0#

Signal Name	Type	Description
HIT#	I/O AGTL+	**Hit**: This signal indicates that a caching agent holds an unmodified version of the requested line. HIT# is also driven in conjunction with HITM# by the target to extend the snoop window.
HITM#	I/O AGTL+	**Hit Modified**: This signal indicates that a caching agent holds a modified version of the requested line and that this agent assumes responsibility for providing the line. HITM# is also driven in conjunction with HIT# to extend the snoop window.
HLOCK#	I AGTL+	**Host Lock**: All processor bus cycles sampled with the assertion of HLOCK# and ADS#, until the negation of HLOCK# must be atomic (i.e., no HI or PCI snoopable access to system memory are allowed when HLOCK# is asserted by the processor).
HREQ[4:0]#	I/O AGTL+ 2X	**Host Request Command**: These signals define the attributes of the request. HREQ[4:0]# are transferred at 2X rate. They are asserted by the requesting agent during both halves of request phase. In the first half the signals define the transaction type to a level of detail that is sufficient to begin a snoop request. In the second half the signals carry additional information to define the complete transaction type. The transactions supported by the MCH Host bridge are defined in Chapter 5.
HTRDY#	O AGTL+	**Host Target Ready**: This signal indicates that the target of the processor transaction is able to enter the data transfer phase.
PROCHOT#	I/0 AGTL+	**Processor Hot**: This signal informs the chipset when processor Tj>thermal monitor trip point.
RS[2:0]#	I/O AGTL+	**Response Signals:** These signals indicates type of response according to the following: **Encoding — Response Type** **000 — Idle state** **001 — Retry response** **010 — Deferred response** **011 — Reserved (not driven by MCH)** **100 — Hard Failure (not driven by MCH)** **101 — No data response** **110 — Implicit Writeback** **111 — Normal data response**

The following is the list of processor bus interface signals that are **not** supported by the MCH:

Signal Name Not Supported	Function Not Supported	Thus, MCH Does Not Support
AP[1:0]#	Address Bus Parity	Parity protection on address bus
DP[3:0]#	Data Parity	Data parity errors on host interface
HA[35:32]	Upper Address Bits	Only supports a 4-GB system address space
RSP#	Response (RS) parity	Response parity errors on host interface
IERR#	Processor Internal Error	Responding to processor internal error
BINIT#	Bus Initialization Signal	Reset of the Host Bus state machines.
MCERR#	Machine Check Error	Signaling or recognition of Machine Check Error

2.2 Memory Interface

2.2.1 DDR DRAM Interface A

The following DDR signals are for DDR channel A.

Signal Name	Type	Description
SCMDCLK_A[5:0]	O SSTL_2	**Differential DDR Clock**: SCMDCLK_Ax and SCMDCLK_Ax# pairs are differential clock outputs. The crossing of the positive edge of SCMDCLK_Ax and the negative edge of SCMDCLK_Ax# is used to sample the address and control signals on the DRAM. There are three pairs to each DIMM.
SCMDCLK_A[5:0]#	O SSTL_2	**Complementary Differential DDR Clock**: These are the complementary Differential DDR Clock signals.
SCS_A[3:0]#	O SSTL_2	**Chip Select:** These signals select particular DRAM components during the active state. There is one SCS_A# for each DRAM row, toggled on the positive edge of SCMDCLK_A.
SMAA_A[12:0]	O SSTL_2	**Memory Address:** These signals are used to provide the multiplexed row and column address to the DRAM.
SBA_A[1:0]	O SSTL_2	**Bank Select (Bank Address):** These signals define which banks are selected within each DRAM row. Bank select and memory address signals combine to address every possible location within an DRAM device.
SRAS_A#	O SSTL_2	**Row Address Strobe:** This signal is used with SCAS_A# and SWE_A# (along with SCS_A#) to define the DRAM commands.
SCAS_A#	O SSTL_2	**Column Address Strobe:** This signal is used with SRAS_A# and SWE_A# (along with SCS_A#) to define the DRAM commands.
SWE_A#	O SSTL_2	**Write Enable:** This signal is used with SCAS_A# and SRAS_A# (along with SCS_A#) to define the DRAM commands.
SDQ_A[63:0]	I/O SSTL_2	**Data Lines:** SDQ_A signals interface to the DRAM data bus.
SDQS_A[8:0]	I/O SSTL_2	**Data Strobes:** Data strobes are used for capturing data. During writes, SDQS_A is centered in data. During reads, SDQS_A is edge aligned with data. The following list matches the data strobe with the data bytes. **Data StrobesData Bytes:** • **SDQS_A8SECC_A[7:0]** • **SDQS_A7SDQ_A[63:56]** • **SDQS_A6SDQ_A[55:48]** • **SDQS_A5SDQ_A[47:40]** • **SDQS_A4SDQ_A[39:32]** • **SDQS_A3SDQ_A[31:24]** • **SDQS_A2SDQ_A[23:16]** • **SDQS_A1SDQ_A[15:8]** • **SDQS_A0SDQ_A[7:0]**
SCKE_A[3:0]	O SSTL_2	**Clock Enable:** SCKE_A is used to initialize DDR DRAM during power-up and to place all DRAM rows into and out of self-refresh during Suspend-to-RAM. SCKE_A is also used to dynamically power down inactive DRAM rows. There is one SCKE_A per DRAM row, toggled on the positive edge of SCMDCLK_A.
SECC_A[7:0]	I/O SSTL-2	**ECC Data bits**: These signals provide the 8-bit ECC data, running at 2X data rate. The data is source synchronous using the DQS Strobes.

2.2.2 DDR DRAM Interface B

The following DDR signals are for DDR channel B.

Signal Name	Type	Description
SCMDCLK_B[5:0]	O SSTL_2	**Differential DDR Clock**: SCMDCLK_Bx and SCMDCLK_Bx# pairs are differential clock outputs. The crossing of the positive edge of SCMDCLK_Bx and the negative edge of SCMDCLK_Bx# is used to sample the address and control signals on the DRAM. There are three pairs to each DIMM.
SCMDCLK_B[5:0]#	O SSTL_2	**Complementary Differential DDR Clock**: These are the complementary differential DDR Clock signals.
SCS_B[3:0]#	O SSTL_2	**Chip Select:** These signals select particular DRAM components during the active state. There is one SCS_B# for each DRAM row, toggled on the positive edge of SCMDCLK_B.
SMAA_B[12:0]	O SSTL_2	**Memory Address:** These signals are used to provide the multiplexed row and column address to the DRAM.
SBA_B[1:0]	O SSTL_2	**Bank Select (Bank Address):** These signals define which banks are selected within each DRAM row. Bank select and memory address signals combine to address every possible location within an DRAM device.
SRAS_B#	O SSTL_2	**Row Address Strobe:** This signal is used with SCAS_B# and SWE_B# (along with SCS_B#) to define the DRAM commands.
SCAS_B#	O SSTL_2	**Column Address Strobe:** This signal is used with SRAS_B# and SWE_B# (along with SCS_B#) to define the DRAM commands.
SWE_B#	O SSTL_2	**Write Enable:** This signal is used with SCAS_B# and SRAS_B# (along with SCS_B#) to define the DRAM commands.
SDQ_B[63:0]	I/O SSTL_2	**Data Lines:** SDQ_B signals interface to the DRAM data bus.
SDQS_B[8:0]	I/O SSTL_2	**Data Strobes:** Data strobes are used for capturing data. During writes, SDQS_B is centered in data. During reads, SDQS_B is edge aligned with data. The following list matches the data strobe with the data bytes. **Data StrobesData Bytes:** • **SDQS_B8SECC_B[7:0]** • **SDQS_B7SDQ_B[63:56]** • **SDQS_B6SDQ_B[55:48]** • **SDQS_B5SDQ_B[47:40]** • **SDQS_B4SDQ_B[39:32]** • **SDQS_B3SDQ_B[31:24]** • **SDQS_B2SDQ_B[23:16]** • **SDQS_B1SDQ_B[15:8]** • **SDQS_B0SDQ_B[7:0]**
SCKE_B[3:0]	O SSTL_2	**Clock Enable:** SCKE_B is used to initialize DDR DRAM during power-up and to place all DRAM rows into and out of self-refresh during Suspend-to-RAM. SCKE_B is also used to dynamically power down inactive DRAM rows. There is one SCKE_B per DRAM row, toggled on the positive edge of SCMDCLK_B.
SECC_B[7:0]	I/O SSTL-2	**ECC Data bits**: These signals provide the 8-bit ECC data, running at 2X data rate. The data is source synchronous using the DQS Strobes.

2.3 Hub Interface

Package/Signal Name	Type	Description
HI[10:0]	I/O sts HI15	**Packet Data:** HI[10:0] are the data signals used for HI read and write operations.
HISTRS	I/O sts HI15	**Packet Strobe:** HISTRS is one of two differential strobe signals used to transmit or receive packet data over HI.
HISTRF	I/O sts HI15	**Packet Strobe Complement:** HISTRF is one of two differential strobe signals used to transmit or receive packet data over HI.

2.4 CSA Interface

Package/ Signal Name	Type	Description
CI[10:0]	I/O sts HI15	**Packet Data:** CI[10:0] are the data signals used for CI read and write operations.
CISTRS	I/O sts HI15	**Packet Strobe:** CISTRS is one of two differential strobe signals used to transmit or receive packet data over CI.
CISTRF	I/O sts HI15	**Packet Strobe Complement:** CISTRF is one of two differential strobe signals used to transmit or receive packet data over CI.

2.5 Clocks, Reset, and Miscellaneous

Signal Name	Type	Description
TESTP[3:0]	O 3.3 V GPIO	**Test Point:** These signals are used as part the XOR/ALL Z test chain and should be routed to a VIA for XOR testing.
TESTP[29:4]	O SSTL_2	**Test Point:** These signals route to pull-up for XOR/ALL Z test chain usage.
TESTP[96:30]	I AGP	**Test Point:** These signals are used as part the XOR/ALL Z test chain and should be routed to a VIA for XOR testing.
HCLKP HCLKN	I CMOS	**Differential Host Clock In:** These pins receive a low-voltage differential host clock from the external clock synthesizer. This clock is used by all of the MCH logic that is in the Host clock domain. 0.7 V
GCLKIN	I LVTTL (3.3 V)	**66 MHz Clock In:**. This pin receives a 66 MHz clock from the clock synthesizer. This clock is used by PCI-X, PCI and HI clock domains. Note that this clock input is required to be 3.3 V tolerant.

Signal Name	Type	Description
RSTIN#	I LVTTL (3.3 V)	**Reset In:** When asserted, this signal asynchronously resets the MCH logic. This signal is connected to the PCIRST# output of the ICH. All PCI output and bi-directional signals will also tri-state compliant to PCI Revision 2.0 and 2.1 specifications. This input should have a Schmitt trigger to avoid spurious resets. Note that this input needs to be 3.3 V tolerant.
PWROK	I LVTTL (3.3 V)	**Power OK:** When asserted, PWROK is an indication to the MCH that the core power and GCLKIN have been stable for at least 10 µs.
EXTTS#	I LVTTL (3.3 V)	**External Thermal Sensor Input**: EXTTS# is an open-drain signal indicating an Over-Temp condition in the platform. This signal should remains asserted for as long as the Over-temp Condition exists. This input pin can be programmed to activate hardware management of memory reads and writes and/or trigger software interrupts.

2.6 RCOMP, VREF, and VSWING

Signal Name	Type	Description
HDVREF[1:0]	I	**Host Data Reference Voltage:** HDVREF[1:0] are reference voltage inputs for the data signals of the host AGTL+ interface.
HDRCOMP	I/O CMOS	**Host RCOMP:** HDRCOMP is used to calibrate the host AGTL+ I/O buffers.
HDSWING	I	**Host Voltage Swing:** These signals provide a reference voltage used by the FSB RCOMP circuit.
SMVREF_A	I	**Memory Reference Voltage for Channel A:** Reference voltage input for system memory interface.
SMXRCOMPVOL	I	**Memory RCOMP for Channel A:** This signal is used to Calibrate V_{OL}.
SMXRCOMPVOH	I	**Memory RCOMP for Channel A**: This signal is used to Calibrate V_{OH}.
SMXRCOMP	I/O CMOS	**Memory RCOMP for Channel A:** This signal is used to calibrate the memory I/O buffers.
SMVREF_B	I	**Memory Reference Voltage for Channel B:** This signal is a reference voltage input for System Memory Interface.
SMYRCOMPVOL	I	**Memory RCOMP for Channel B**: This signal is used to Calibrate V_{OL}.
SMYRCOMPVOH	I	**Memory RCOMP for Channel B**: This signal is used to Calibrate V_{OH}.
SMYRCOMP	I/O CMOS	**Memory RCOMP for Channel B:** This signal is used to calibrate the memory I/O buffers.
GVREF	I	**Reference Voltage:** This signal provides a 0.75V reference voltage.
HI_VREF	I	**HI Reference:** This signal provides the reference voltage input for the HI interface.
HI_RCOMP	I/O CMOS	**Compensation for HI:** This signal is used to calibrate the HI I/O buffers.
HI_SWING	I	**HI Voltage Swing:** This signal provides a reference voltage used by the HI_RCOMP circuit.
CI_VREF	I	**CSA Reference:** This signal provides the reference voltage input for the CSA interface.
CI_RCOMP	I/O CMOS	**Compensation for CSA:** This signal is used to calibrate the CSA I/O buffers.
CI_SWING	I	**CSA Voltage Swing:** This signal provides a reference voltage used by the CI_RCOMP circuit.

NOTE: Reference the *Intel® 875P/Intel® E7210/Intel® 6300ESB Chipset Platform Design Guide* for platform design information.

2.7 Power and Ground Signals

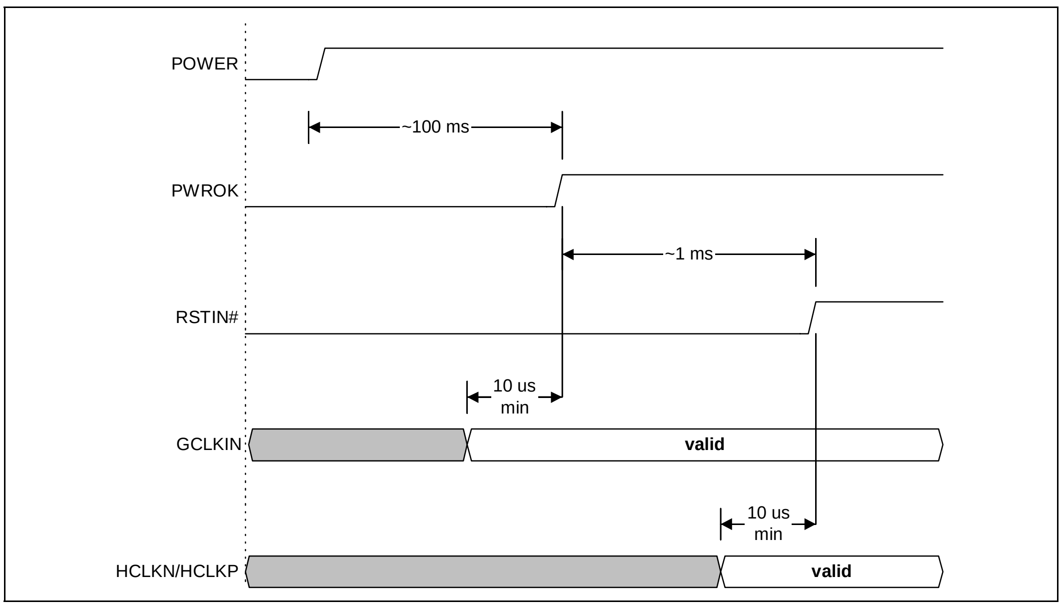
Signal Name	Description
VCC	**VCC Supply:** This is the 1.5 V core.
VSS	**Gnd Supply**
VCCA_FSB	**Analog VCC for the Host PLL:** This 1.5 V supply requires special filtering. Refer to the *Intel® 875P/Intel® E7210/Intel® 6300ESB Chipset Platform Design Guide* for details.
VTT	**VTT Supply:** VTT is a FSB supply and has a range of 1.1 V–1.55 V.
VCC_HI	**Hub VCC Power:** This is a 1.5 V supply for the hub interface and CSA interface.
VCC_33	**3.3 V Supply:** This supply is used for XOR Chain testing.
VCC_DDR	**VCC for System Memory:** VCC_DDR is 2.6 V for DDR.
VCCA_DDR	**Analog VCC for System Memory:** This signal is a 1.5 V supply for DDR. The supply requires special filtering. Refer to the *Intel® 875P/Intel® E7210/Intel® 6300ESB Chipset Platform Design Guide* for details.

2.8 MCH Sequencing Requirements

Power plane and sequencing requirements:

- Clock valid timing:
  - — GCLKIN must be valid at least 10 µs prior to the rising edge of PWROK.
  - — HCLKN/HCLKP must be valid at least 10 µs prior to the rising edge of RSTIN#.

Figure 3. Intel® E7210 Chipset System Clock and Reset Requirements



The MCH uses the rising edge of PWROK to latch straps values. During S3, when power is not valid, the MCH requires that PWROK de-assert and then re-assert when power is valid so that it can properly re-latch the straps.

2.9 Signals Used As Straps

2.9.1 Functional Straps

Signal Name	Strap Name	Description
HA7#	FSB IOQ Depth	The value on HA7# is sampled by all processor bus agents, including the MCH, on the de-asserting edge of CPURST#. **NOTE:** For HA7# the minimum setup time is 4 HCLKs. The minimum hold time is 2 clocks and the maximum hold time is 20 HCLKs. The latched value determines the maximum IOQ depth supported on the processor bus. • **0 (low voltage) = BUS IOQ depth on the bus is 1** • **1 (high voltage) = BUS IOQ depth on the bus is the maximum of 12**

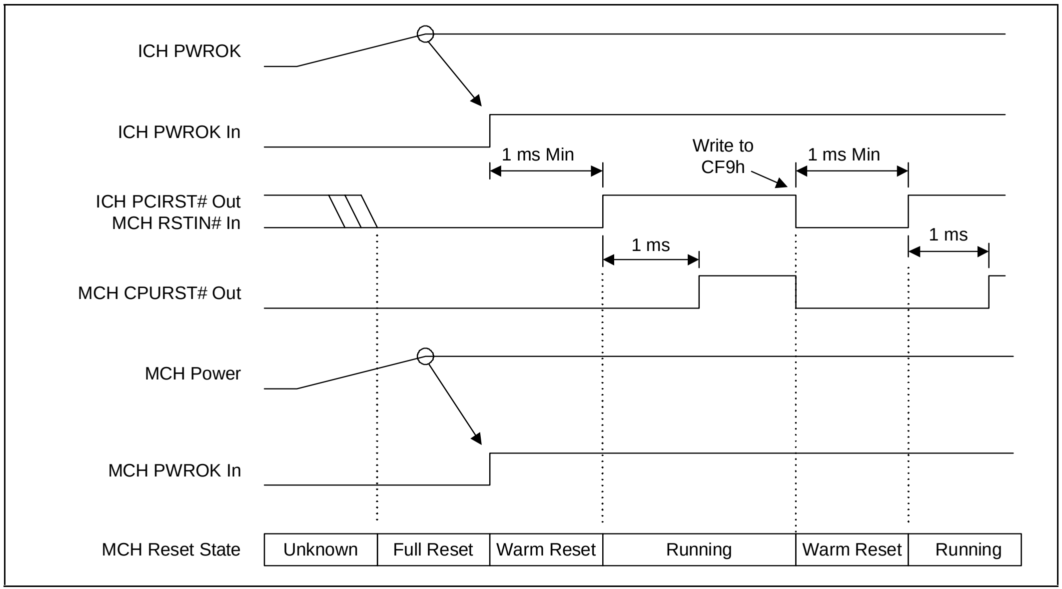
NOTE: All straps, have internal 8 kΩ pull-ups (HA7# has GTL pull-up) enabled during their sampling window. Therefore, a strap that is not connected or not driven by external logic will be sampled high.

2.9.2 Strap Input Signals

Signal Name	Type	Description
BSEL[1:0]	I CMOS	**Core / FSB Frequency (FSBFREQ) Select Strap:** This strap is latched at the rising edge of PWROK. These pins has no default internal pull-up resistor. 00 = Core frequency is 100 MHz, FSB frequency is 400 MHz 01 = Core frequency is 133 MHz, FSB frequency is 533 MHz 10 = Core Frequency is 200 MHz, FSB frequency is 800 MHz 11 = Reserved

2.10 Full and Warm Reset States

Figure 4. Full and Warm Reset Waveforms



All register bits assume their default values during full reset. PCIRST# resets all internal flops and state machines (except for a few configuration register bits). A full reset occurs when PCIRST# (MCH RSTIN#) is asserted and PWROK is deasserted (see Table 3). A warm reset occurs when PCIRST# (MCH RSTIN#) is asserted and PWROK is also asserted.

Table 3. Full and Warm Reset States

Reset State	RSTIN#	PWROK
Full Reset	L	L
Warm Reset	L	H
Does Not Occur	H	L
Normal Operation	H	H

§

Register Description 3

The MCH contains two sets of software accessible registers, accessed via the host processor I/O address space:

- Control registers I/O mapped into the processor I/O space that controls access to PCI configuration space.
- Internal configuration registers residing within the MCH are partitioned into logical device register sets ("logical" since they reside within a single physical device). The first register set is dedicated to host-hub interface functionality (controls PCI bus 0, i.e., DRAM configuration, other chipset operating parameters, and optional features). The second register block is dedicated to host-CSA control.

The MCH supports PCI configuration space accesses using the mechanism denoted as Configuration Mechanism 1 in the PCI specification. The MCH internal registers (both I/O mapped and configuration registers) are accessible by the host processor. The registers can be accessed as Byte, Word (16-bit), or DWord (32-bit) quantities, with the exception of CONFIG_ADDRESS which can only be accessed as a DWord. All multi-byte numeric fields use "little-endian" ordering (i.e., Lower addresses contain the least significant parts of the field).

3.1 Register Terminology

Term	Description
RO	**Read Only**. If a register is read only, writes to this register have no effect.
R/W	**Read/Write**. A register with this attribute can be read and written.
R/W/L	**Read/Write/Lock**. A register with this attribute can be read, written, and Locked.
R/WC	**Read/Write Clear**. A register bit with this attribute can be read and written. However, a write of a 1 clears (sets to 0) the corresponding bit and a write of a 0 has no effect.
R/WO	**Read/Write Once.** A register bit with this attribute can be written to only once after power up. After the first write, the bit becomes read only.
L	**Lock.** A register bit with this attribute becomes Read Only after a lock bit is set.
Reserved Bits	Some of the MCH registers described in this section contain reserved bits. These bits are labeled "Reserved". Software must deal correctly with fields that are reserved. On reads, software must use appropriate masks to extract the defined bits and not rely on reserved bits being any particular value. On writes, software must ensure that the values of reserved bit positions are preserved. That is, the values of reserved bit positions must first be read, merged with the new values for other bit positions and then written back. Note that software does not need to perform a read-merge-write operation for the Configuration Address (CONFIG_ADDRESS) register.
Reserved Registers	In addition to reserved bits within a register, the MCH contains address locations in the configuration space of the Host-HI bridge entity that are marked either "Reserved" or "Intel Reserved". The MCH responds to accesses to "Reserved" address locations by completing the host cycle. When a "Reserved" register location is read, a zero value is returned. ("Reserved" registers can be 8, 16, or 32 bits in size). Writes to "Reserved" registers have no effect on the MCH. Registers that are marked as "Intel Reserved" must not be modified by system software. Writes to "Intel Reserved" registers may cause system failure. Reads to "Intel Reserved" registers may return a non-zero value.

Term	Description
Default Value upon a Reset	Upon a reset, the MCH sets all of its internal configuration registers to predetermined default states. Some register values at reset are determined by external strapping options. The default state represents the minimum functionality feature set required to successfully bring up the system. Hence, it does not represent the optimal system configuration. It is the responsibility of the system initialization software (usually BIOS) to properly determine the DRAM configurations, operating parameters and optional system features that are applicable, and to program the MCH registers accordingly.

3.2 Platform Configuration Structure

In some previous chipsets, the "MCH" and the "I/O Controller Hub (ICH)" were physically connected by PCI bus 0. From a configuration standpoint, both components appeared to be on PCI bus 0 which was also the system's primary PCI expansion bus. The MCH contained two PCI devices while the ICHx was considered one PCI device with multiple functions.

In the Intel E7210 chipset platform the configuration structure is significantly different. The MCH and the ICH are physically connected by the hub interface; thus, from a configuration standpoint, the hub interface is logically PCI bus 0. As a result, all devices internal to the MCH and ICH appear to be on PCI bus 0. The system's primary PCI expansion bus is physically attached to the ICH and, from a configuration perspective, appears to be a hierarchical PCI bus behind a PCI-to-PCI bridge; therefore, it has a programmable PCI Bus number. Note that the primary PCI bus is referred to as PCI_A in this document and is **not** PCI bus 0 from a configuration standpoint.

The MCH contains three PCI devices within a single physical component. The configuration registers for the three devices are mapped as devices residing on PCI bus 0.

- **Device 0:** Host-HI bridge/DRAM controller. Logically, this appears as a PCI device residing on PCI bus 0. Physically, Device 0 contains the standard PCI registers, DRAM registers, configuration for HI, and other MCH specific registers.
- **Device 3**: CSA Port. This device appears as a Virtual PCI-CSA (PCI-to-PCI) bridge device.
- **Device 6:** Function 0: Overflow Device. The purpose of this device is to provide additional configuration register space for Device 0.

Table 4 shows the Device # assignment for the various internal MCH devices.

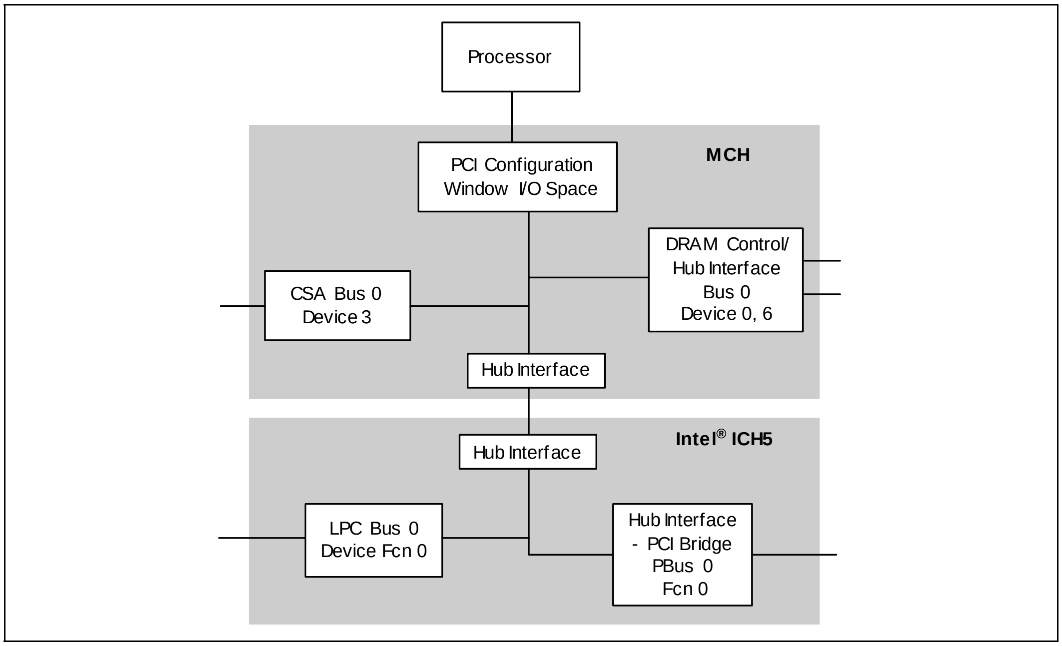
Table 4. Internal MCH Device Assignment

MCH Function	Bus #0, Device #
DRAM Controller/8-bit HI Controller	Device 0
Intergrated GBE (CSA)	Device 3
Overflow	Device 6

Logically, the ICH appears as multiple PCI devices within a single physical component also residing on PCI bus 0. One of the ICH devices is a PCI-to-PCI bridge. Logically, the primary side of the bridge resides on PCI 0 while the secondary side is the standard PCI expansion bus.

Note: A physical PCI bus 0 does not exist and that HI and the internal devices in the MCH and ICH logically constitute PCI Bus 0 to configuration software.

Figure 5. Conceptual Intel® E7210 Chipset Platform PCI Configuration Diagram



3.3 Routing Configuration Accesses

The MCH supports two bus interfaces: HI and PCI. PCI configuration cycles are selectively routed to one of these interfaces. The MCH is responsible for routing PCI configuration cycles to the proper interface. PCI configuration cycles to ICH internal devices and Primary PCI (including downstream devices) are routed to the ICH via HI.

A detailed description of the mechanism for translating processor I/O bus cycles to configuration cycles on one of the buses is described in the following sections.

3.3.1 Standard PCI Bus Configuration Mechanism

The PCI Bus defines a slot based "configuration space" that allows each device to contain up to eight functions with each function containing up to 256, 8-bit configuration registers. The PCI specification defines two bus cycles to access the PCI configuration space: Configuration Read and Configuration Write. Memory and I/O spaces are supported directly by the processor. Configuration space is supported by a mapping mechanism implemented within the MCH. The PCI 2.3 specification defines the configuration mechanism to access configuration space. The configuration access mechanism makes use of the CONFIG_ADDRESS Register (at I/O address 0CF8h though 0CFBh) and CONFIG_DATA Register (at I/O address 0CFCh through 0CFFh). To reference a configuration register a DWord I/O write cycle is used to place a value into CONFIG_ADDRESS that specifies the PCI bus, the device on that bus, the function within the device, and a specific configuration register of the device function being accessed. CONFIG_ADDRESS[31] must be 1 to enable a configuration cycle. CONFIG_DATA then becomes a window into the four bytes of configuration space specified by the contents of CONFIG_ADDRESS. Any read or write to CONFIG_DATA will result in the MCH translating the CONFIG_ADDRESS into the appropriate configuration cycle.

The MCH is responsible for translating and routing the processor's I/O accesses to the CONFIG_ADDRESS and CONFIG_DATA registers to internal MCH configuration registers or HI.

3.3.2 PCI Bus 0 Configuration Mechanism

The MCH decodes the Bus Number (bits 23:16) and the Device Number fields of the CONFIG_ADDRESS register. If the Bus Number field of CONFIG_ADDRESS is 0, the configuration cycle is targeting a PCI Bus 0 device. The Host-HI bridge entity within the MCH is hardwired as Device 0 on PCI Bus 0. Device 6 contains device configuration registers.

3.3.3 Primary PCI and Downstream Configuration Mechanism

If the Bus Number in the CONFIG_ADDRESS is non-zero the MCH will generate a Type 1 HI configuration cycle. A[1:0] of the HI request packet for the Type 1 configuration cycle will be 01. Bits 31:2 of the CONFIG_ADDRESS register will be translated to the A[31:2] field of the HI request packet of the configuration cycle. This HI configuration cycle will be sent over HI.

If the cycle is forwarded to the ICH via HI, the ICH compares the non-zero Bus Number with the Secondary Bus Number and Subordinate Bus Number Registers of its PCI-to-PCI bridges to determine if the configuration cycle is meant for Primary PCI, one of the ICH's HIs, or a downstream PCI bus.

3.4 I/O Mapped Registers

The MCH contains two registers that reside in the processor I/O address space: the Configuration Address (CONFIG_ADDRESS) Register and the Configuration Data (CONFIG_DATA) Register. The Configuration Address Register enables/disables the configuration space and determines what portion of configuration space is visible through the Configuration Data window.

3.4.1 CONFIG_ADDRESS—Configuration Address Register

I/O Address: 0CF8h Accessed as a DWord
Default Value: 00000000h
Access: R/W
Size: 32 bits

CONFIG_ADDRESS is a 32-bit register that can be accessed only as a DWord. A Byte or Word reference will "pass through" the Configuration Address Register and HI onto the PCI_A bus as an I/O cycle. The CONFIG_ADDRESS register contains the Bus Number, Device Number, Function Number, and Register Number for which a subsequent configuration access is intended.

Bit	Descriptions
31	**Configuration Enable (CFGE).** 1 = Enable 0 = Disable
30:24	Reserved
23:16	**Bus Number.** When the Bus Number is programmed to 00h, the target of the configuration cycle is a HI agent (MCH, ICH, etc.). The configuration cycle is forwarded to HI if the Bus Number is programmed to 00h and the MCH is not the target (i.e., device number is not equal to 0, 1, 2, 3, 6). If the Bus Number is non-zero a HI Type 1 configuration cycle is generated.

Bit	Descriptions
15:11	**Device Number.** This field selects one agent on the PCI bus selected by the Bus Number. When the Bus Number field is 00, the MCH decodes the Device Number field. The MCH is always Device Number 0 for the Host-HI bridge entity. Therefore, when the Bus Number =0 and the Device Number equals 0, 1, 2, 3, 6, the internal MCH devices are selected. For Bus Numbers resulting in HI configuration cycles, the MCH propagates the Device Number field as A[15:11].
10:8	**Function Number.** This field is mapped to A[10:8] during HI configuration cycles. This allows the configuration registers of a particular function in a multi-function device to be accessed. The MCH ignores configuration cycles to its internal Devices if the function number is not equal to 0.
7:2	**Register Number.** This field selects one register within a particular Bus, Device, and Function as specified by the other fields in the Configuration Address Register. This field is mapped to A[7:2] during HI configuration cycles.
1:0	Reserved

3.4.2 CONFIG_DATA—Configuration Data Register

I/O Address: 0CFCh
Default Value: 00000000h
Access: R/W
Size: 32 bits

CONFIG_DATA is a 32-bit read/write window into configuration space. The portion of configuration space that is referenced by CONFIG_DATA is determined by the contents of CONFIG_ADDRESS.

Bit	Descriptions
31:0	**Configuration Data Window (CDW).** If bit 31 of CONFIG_ADDRESS is 1, any I/O access to the CONFIG_DATA register will be mapped to configuration space using the contents of CONFIG_ADDRESS.

3.5 DRAM Controller/Host-Hub Interface Device Registers (Device 0)

This section contains the DRAM Controller and Host-Hub Interface PCI configuration registers listed in order of ascending offset address. The register address map is shown in Table 5.

Table 5. DRAM Controller/Host-Hub Interface Device Register Address Map (Device 0)

Address Offset	Register Symbol	Register Name	Default Value	Access
00–01h	VID	Vendor Identification	8086h	RO
02–03h	DID	Device Identification	2578h	RO
04–05h	PCICMD	PCI Command	0006h	RO, R/W
06–07h	PCISTS	PCI Status	0090h	RO, R/WC
08h	RID	Revision Identification	See register description	RO
09h	—	Intel Reserved	—	—
0Ah	SUBC	Sub-Class Code	00h	RO
0Bh	BCC	Base Class Code	06h	RO

Table 5. DRAM Controller/Host-Hub Interface Device Register Address Map (Device 0) (Continued)

Address Offset	Register Symbol	Register Name	Default Value	Access
0C	—	Intel Reserved	—	—
0Dh	MLT	Master Latency Timer	00h	RO
0Eh	HDR	Header Type	00h	RO
0Fh	—	Intel Reserved	—	—
10–13h	—	Intel Reserved	—	—
14–2Bh	—	Intel Reserved	—	—
2C–2Dh	SVID	Subsystem Vendor Identification	0000h	R/WO
2E–2Fh	SID	Subsystem Identification	0000h	R/WO
30–33h	—	Intel Reserved	—	—
34h	CAPPTR	Capabilities Pointer	E4h	RO
35–50h	—	Intel Reserved	—	RO
51h	—	Intel Reserved	—	—
52h	—	Intel Reserved	—	—
53h	CSABCONT	CSA Basic Control	0000_000sb	RO, R/W
54–57h		Intel Reserved		
58–5Bh	EAP	DRAM Error Data Register	undefined	RO
5Ch	DERRSYN	DRAM Error Syndrome	undefined	RO
5Dh	DES	DRAM Error Status	undefined	RO
5E–5Fh	—	Intel Reserved	—	—
60h	FPLLCONT	FPLL Clock Control	00h	R/W, RO
61–89h	—	Intel Reserved	—	—
90h	PAM0	Programmable Attribute Map 0	00h	RO, R/W
91h	PAM1	Programmable Attribute Map 1	00h	RO, R/W
92h	PAM2	Programmable Attribute Map 2	00h	RO, R/W
93h	PAM3	Programmable Attribute Map 3	00h	RO, R/W
94h	PAM4	Programmable Attribute Map 4	00h	RO, R/W
95h	PAM5	Programmable Attribute Map 5	00h	RO, R/W
96h	PAM6	Programmable Attribute Map 6	00h	RO, R/W
97h	FDHC	Fixed DRAM Hole Control	00h	RO, R/W
98–9Ch	—	Intel Reserved		
9Dh	SMRAM	System Management RAM Control	02h	RO, R/W, L
9Eh	ESMRAMC	Extended System Management RAM Control	38h	RO, R/W, RWC, L
9Fh	—	Intel Reserved	—	—
A0–A3h	—	Intel Reserved	—	—
A4–A7h	—	Intel Reserved	—	—
A8–ABh	—	Intel Reserved	—	—
AC–AFh	—	Intel Reserved	—	—
B0–B3h	—	Intel Reserved	—	—
B4h	—	Intel Reserved	—	—

Table 5. DRAM Controller/Host-Hub Interface Device Register Address Map (Device 0) (Continued)

Address Offset	Register Symbol	Register Name	Default Value	Access
B5–B7h	—	Intel Reserved	—	—
B8–BBh	—	Intel Reserved	—	—
BCh	—	Intel Reserved	—	—
BDh	—	Intel Reserved	—	—
BE–C3h	—	Intel Reserved	—	—
C4–C5h	TOUD	Top of Used DRAM	0400h	RO, R/W
C6–C7h	MCHCFG	MCH Configuration	0000h	R/WO, RO, R/W
C8–C9h	ERRSTS	Error Status	0000h	R/WC
CA–CBh	ERRCMD	Error Command	0000h	RO, R/W
CC–CDh	SMICMD	SMI Command	0000h	RO, R/W
CE–CFh	SCICMD	SCI Command	0000h	RO, R/W
D0–DDh	—	Intel Reserved	—	—
DE–DFh	SKPD	Scratchpad Data	0000h	R/W
E0–E3h	—	Intel Reserved	—	—
E4–E9h	CAPREG	Capability Identification	00_0106_A009h	RO
EA–FFh	—	Intel Reserved	—	—

3.5.1 VID—Vendor Identification Register (Device 0)

Address Offset: 00–01h
Default Value: 8086h
Access: RO
Size: 16 bits

The VID Register contains the vendor identification number. This 16-bit register, combined with the Device Identification Register, uniquely identify any PCI device.

Bit	Descriptions
15:0	**Vendor Identification (VID)—RO.** This register field contains the PCI standard identification for Intel, 8086h.

3.5.2 DID—Device Identification Register (Device 0)

Address Offset: 02–03h
Default Value: 2578h
Access: RO
Size: 16 bits

This 16-bit register combined with the Vendor Identification register uniquely identifies any PCI device.

Bit	Descriptions
15:0	**Device Identification Number (DID)—RO.** This is a 16-bit value assigned to the MCH Host-HI bridge Function 0.

3.5.3 PCICMD—PCI Command Register (Device 0)

Address Offset: 04–05h
Default Value: 0006h
Access: RO, R/W
Size: 16 bits

Since MCH Device 0 does not physically reside on PCI_A, many of the bits are not implemented.

Bit	Descriptions
15:10	Reserved
9	**Fast Back-to-Back Enable (FB2B)—RO.** Hardwired to 0. This bit controls whether or not the master can do fast back-to-back write. Since Device 0 is strictly a target this bit is not implemented and hardwired to 0.
8	**SERR Enable (SERRE)—R/W.** This bit is a global enable bit for Device 0 SERR messaging. The MCH does not have an SERR signal. The MCH communicates the SERR condition by sending an SERR message over HI to the ICH. 1 = MCH is enabled to generate SERR messages over HI for specific Device 0 error conditions that are individually enabled in the ERRCMD register. The error status is reported in the ERRSTS and PCISTS registers. 0 = The SERR message is not generated by the MCH for Device 0. Note that this bit only controls SERR messaging for the Device 0. Device 1has its own SERRE bits to control error reporting for error conditions occurring on their respective devices. The control bits are used in a logical OR manner to enable the SERR HI message mechanism.
7	**Address/Data Stepping Enable (ADSTEP)—RO.** Hardwired to 0.
6	**Parity Error Enable (PERRE)—RO.** Hardwired to 0. PERR# is not implemented by the MCH.
5	**VGA Palette Snoop Enable (VGASNOOP)—RO.** Hardwired to 0.
4	**Memory Write and Invalidate Enable (MWIE)—RO.** Hardwired to 0. The MCH will never issue memory write and invalidate commands.
3	**Special Cycle Enable (SCE)—RO.** Hardwired to 0.
2	**Bus Master Enable (BME)—RO.** Hardwired to 1. The MCH is always enabled as a master on HI.
1	**Memory Access Enable (MAE)—RO.** Hardwired to 1. The MCH always allows access to main memory.
0	**I/O Access Enable (IOAE)—RO.** Hardwired to 0.

3.5.4 PCISTS—PCI Status Register (Device 0)

Address Offset: 06–07h
Default Value: 0090h
Access: RO, R/WC
Size: 16 bits

PCISTS is a 16-bit status register that reports the occurrence of error events on Device 0’s PCI interface. Since MCH Device 0 does not physically reside on PCI_A many of the bits are not implemented.

Bit	Descriptions
15	**Detected Parity Error (DPE)—RO.** Hardwired to 0. Writes to this bit position have no effect.
14	**Signaled System Error (SSE)—R/WC.** 0 = Software sets this bit to 0 by writing a 1 to this bit. 1 = MCH Device 0 generated an SERR message over HI for any enabled Device 0 error condition. Device 0 error conditions are enabled in the PCICMD and ERRCMD registers. Device 0 error flags are read/reset from the PCISTS or ERRSTS registers.

Bit	Descriptions
13	**Received Master Abort Status (RMAS)—R/WC.** 0 = Software sets this bit to 0 by writing a 1 to this bit. 1 = MCH generated a HI request that receives a Master Abort completion packet or Master Abort Special Cycle.
12	**Received Target Abort Status (RTAS)—R/WC.** 0 = Software sets this bit to 0 by writing a 1 to this bit. 1 = MCH generated a HI request that receives a Target Abort completion packet or Target Abort Special Cycle.
11	**Signaled Target Abort Status (STAS)—RO.** Hardwired to 0. The MCH will not generate a Target Abort HI completion packet or Special Cycle.
10:9	**DEVSEL Timing (DEVT)—RO.** Hardwired to 00. Device 0 does not physically connect to PCI_A. These bits are set to 00 (fast decode) so that optimum DEVSEL timing for PCI_A is not limited by the MCH.
8	**Master Data Parity Error Detected (DPD)—RO.** Hardwired to 0. PERR signaling and messaging are not implemented by the MCH.
7	**Fast Back-to-Back (FB2B)—RO.** Hardwired to 1. Device 0 does not physically connect to PCI_A. This bit is set to 1 (indicating fast back-to-back capability) so that the optimum setting for PCI_A is not limited by the MCH.
6:5	Reserved
4	**Capability List (CLIST)—RO.** Hardwired to 1 to indicate to the configuration software that this device/function implements a list of new capabilities. A list of new capabilities is accessed via register CAPPTR at configuration address offset 34h.
3:0	Reserved

3.5.5 RID—Revision Identification Register (Device 0)

Address Offset: 08h
Default Value: See following table
Access: RO
Size: 8 bits

This register contains the revision number of the MCH Device 0.

Bit	Descriptions
7:0	**Revision Identification Number (RID)—RO.** This is an 8-bit value that indicates the revision identification number for the MCH Device 0. 02h = A-2 Stepping

3.5.6 SUBC—Sub-Class Code Register (Device 0)

Address Offset: 0Ah
Default Value: 00h
Access: RO
Size: 8 bits

This register contains the Sub-Class Code for the MCH Device 0.

Bit	Descriptions
7:0	**Sub-Class Code (SUBC)—RO.** This is an 8-bit value that indicates the category of bridge for the MCH Device 0. 00h = Host bridge.

3.5.7 BCC—Base Class Code Register (Device 0)

Address Offset: 0Bh
Default Value: 06h
Access: RO
Size: 8 bits

This register contains the Base Class Code of the MCH Device 0.

Bit	Descriptions
7:0	**Base Class Code (BASEC)—RO.** This is an 8-bit value that indicates the Base Class Code for the MCH Device 0. 06h = Bridge device.

3.5.8 MLT—Master Latency Timer Register (Device 0)

Address Offset: 0Dh
Default Value: 00h
Access: RO
Size: 8 bits

Device 0 in the MCH is not a PCI master. Therefore, this register is not implemented.

Bit	Descriptions
7:0	Reserved

3.5.9 HDR—Header Type Register (Device 0)

Address Offset: 0Eh
Default Value: 00h
Access: RO
Size: 8 bits

This register identifies the header layout of the configuration space. No physical register exists at this location.

Bit	Descriptions
7:0	**PCI Header (HDR)—RO.** This field always returns 0 to indicate that the MCH is a single-function device with standard header layout.

3.5.10 SVID—Subsystem Vendor Identification Register (Device 0)

Address Offset: 2C–2Dh
Default Value: 0000h
Access: R/WO
Size: 16 bits

This value is used to identify the vendor of the subsystem.

Bit	Descriptions
15:0	**Subsystem Vendor ID (SUBVID)—R/WO.** This field should be programmed during boot-up to indicate the vendor of the system board. After it has been written once, it becomes read only.

3.5.11 SID—Subsystem Identification Register (Device 0)

Address Offset: 2E–2Fh
Default Value: 0000h
Access: R/WO
Size: 16 bits

This value is used to identify a particular subsystem.

Bit	Descriptions
15:0	**Subsystem ID (SUBID)—R/WO.** This field should be programmed during BIOS initialization. After it has been written once, it becomes read only.

3.5.12 CAPPTR—Capabilities Pointer Register (Device 0)

Address Offset: 34h
Default Value: E4h
Access: RO
Size: 8 bits

The CAPPTR provides the offset that is the pointer to the location of the first device capability in the capability list.

Bit	Descriptions
7:0	**Capabilities Pointer Address—RO.** This field contains the pointer to the offset of the first capability ID register block. In this case the first capability is the Product-Specific Capability, which is located at offset E4h.

3.5.13 CSABCONT—CSA Basic Control Register (Device 0)

Address Offset: 53h
Default: 0000_000sb (s=Strap value)
Access: R/W, RO
Size: 8 bits

Bit	Description
7:1	Reserved
0	**Device Not Present bit—R/W.** The default is set by the power on strap. The strap is on CI9 of the CSA port and the strap value is latched onPWROK assertion. This bit is read/write so software can completely disable the CSA device, even if it is present. 0 = Device Not Enabled 1 = Device Enabled

3.5.14 EAP—DRAM Error Data Register (Device 0)

Address Offset: 58–5Bh
Default: Undefined
Access: RO
Size: 32 bits
Sticky: No

This register contains the access on which a DRAM ECC error was detected. This register will have an undefined value when no ECC errors have been logged.

Bit	Description
31:12	**Error Address Pointer (EAP)—RO.** This field is used to store the address block of main memory of which an error (single bit or multi-bit error) has occurred. Note that the value of this bit field represents the address of the first single or the first multiple bit error occurrence after the error flag bits in the ERRSTS register have been cleared by software. A multiple bit error will overwrite a single bit error. Once the error flag bits are set as a result of an error, this bit field is locked and does not change as a result of a new error.
11:0	Reserved (RO.

3.5.15 DERRSYN—DRAM Error Syndrome Register (Device 0)

Address Offset: 5Ch
Default: Undefined
Access: RO
Size: 8 bits
Sticky: No

This register will be updated with bit 7 having the highest priority and Bit 0 having the lowest priority. Like EAP, the value in this register represents information about the first single or multi-bit error that has occurred. A multi-bit error will overwrite a single bit error. Below is the priority ordering.

- Multi-Bit ECC Error on QW0 - RO
- Multi-Bit ECC Error on QW1 - RO
- Multi-Bit ECC Error on QW2 - RO
- Multi-Bit ECC Error on QW3 - RO
- Correctable Single-Bit ECC Error on QW0 - RO
- Correctable Single-Bit ECC Error on QW1 - RO
- Correctable Single-Bit ECC Error on QW2 - RO
- Correctable Single-Bit ECC Error on QW3 - RO

This register will have an undefined value when no ECC errors have been logged.

Bit	Description
7:0	**DRAM ECC Syndrome (DECCSYN)—RO.** After a DRAM ECC error on any quadword of the 32-B aligned data chunk, hardware loads this field with a syndrome that describes the set of bits associated with first failing quadword. Note that this field is locked from the time that it is loaded up to the time when the error flag is cleared by software. However, if the first error was a single bit, correctable error, then a subsequent multiple bit error will cause the field to be re-recorded. An error that occurs after the first error and before the error flag has been cleared by software will escape recording.

3.5.16 DES—DRAM Error Status Register (Device 0)

Address Offset: 5Dh
Default: Undefined
Access: RO
Size: 8 bits
Sticky: No

This register will have an undefined value when no ECC errors have been logged.

Bit	Description
7:1	Reserved
0	**Error Channel—RO.** 0 = Error Detected on Channel A. 1 = Error Detected on Channel B.

3.5.17 FPLLCONT— Front-Side Bus PLL Clock Control Register (Device 0)

Address Offset: 60h
Default Value: 00h
Access: R/W, RO
Size: 8 bits

These register bits are used for changing DDR frequency, initializing MCH memory and I/O clocks' WIO DLL delays.

Bit	Descriptions
7:5	Reserved
4	**Memory and Memory I/O DLL Clock Gate (DLLCKGATE)—R/W.** Note that this bit should always be written to before writing to the FPLLSYNC bit. 0 = Writing a 0 cleanly re-enables the memory and memory I/O clocks from the DLL outputs. (default) 1 = Writing a 1 cleanly disables the memory and memory I/O clocks of the chipset core and DDR interface from the DLL outputs.
3:2	Intel Reserved (Default=00)
1	**FSB PLL Sync (FPLLSYNC)—R/W.** 0 = After writing a 1, writing a 0 causes the FSB PLL to synchronize the memory to the processor clock. 1 = Writing a 1 resets the memory clock dividers in the FSB FPLL. This also enables the output of the system memory frequency bits to propagate to the chip and the FPLL.
0	**Memory Clock Gate (GMCLKGATE)—R/W.** Note that this bit should always be written to before writing to the FPLLSYNC bit. 0 = Writing a 0 restarts (enables) the clocks. 1 = Writing a 1 cleanly disables the memory clocks while still enabling the core clocks. The memory clocks can then be programmed with new speed information.

3.5.18 PAM[0:6]—Programmable Attribute Map Registers (Device 0)

Address Offset: 90–96h (PAM0–PAM6)
Default Value: 00h
Attribute: R/W, RO
Size: 8 bits

The MCH allows programmable memory attributes on 13 Legacy memory segments of various sizes in the 768-KB to 1-MB address range. Seven Programmable Attribute Map (PAM) Registers are used to support these features. Cacheability of these areas is controlled via the MTRR registers in the processor. Two bits are used to specify memory attributes for each memory segment. These bits apply to host initiator only access to the PAM areas. MCH will forward to main memory for any PCI, or HI initiated accesses to the PAM areas. These attributes are:

RE **Read Enable.** When RE = 1, the host read accesses to the corresponding memory segment are claimed by the MCH and directed to main memory. Conversely, when RE = 0, the host read accesses are directed to PCI_A.

WE **Write Enable.** When WE = 1, the host write accesses to the corresponding memory segment are claimed by the MCH and directed to main memory. Conversely, when WE = 0, the host write accesses are directed to PCI_A.

The RE and WE attributes permit a memory segment to be read only, write only, read/write, or disabled. For example, if a memory segment has RE = 1 and WE = 0, the segment is read only.

Each PAM register controls two regions, typically 16 KB in size. Each of these regions has a 4-bit field. The four bits that control each region have the same encoding defined in the following table.

Bits [7, 3] Reserved	Bits [6, 2] Reserved	Bits [5, 1] WE	Bits [4, 0] RE	Description
X	X	0	0	Disabled DRAM is disabled and all accesses are directed to the hub interface. The MCH does not respond as a PCI target for any read or write access to this area.
X	X	0	1	Read Only. Reads are forwarded to DRAM and writes are forwarded to the hub interface for termination. This write protects the corresponding memory segment. The MCH will respond as the hub interface target for read accesses but not for any write accesses.
X	X	1	0	Write Only. Writes are forwarded to DRAM and reads are forwarded to the hub interface for termination. The MCH will respond as a hub interface target for write accesses but not for any read accesses.
X	X	1	1	Read/Write. This is the normal operating mode of main memory. Both read and write cycles from the host are claimed by the MCH and forwarded to DRAM. The MCH will respond as a hub interface target for both read and write accesses.

At the time that a HI access to the PAM region occurs, the targeted PAM segment must be programmed to be both readable and writable.

As an example, consider BIOS that is implemented on the expansion bus. During the initialization process, the BIOS can be shadowed in main memory to increase the system performance. When BIOS is shadowed in main memory, it should be copied to the same address location. To shadow the BIOS, the attributes for that address range should be set to write only. The BIOS is shadowed by first doing a read of that address. This read is forwarded to the expansion bus. The host then

does a write of the same address, which is directed to main memory. After the BIOS is shadowed, the attributes for that memory area are set to read only so that all writes are forwarded to the expansion bus. Figure 6 and Table 6 show the PAM registers and the associated attribute bits.

Figure 6. PAM Register Attributes

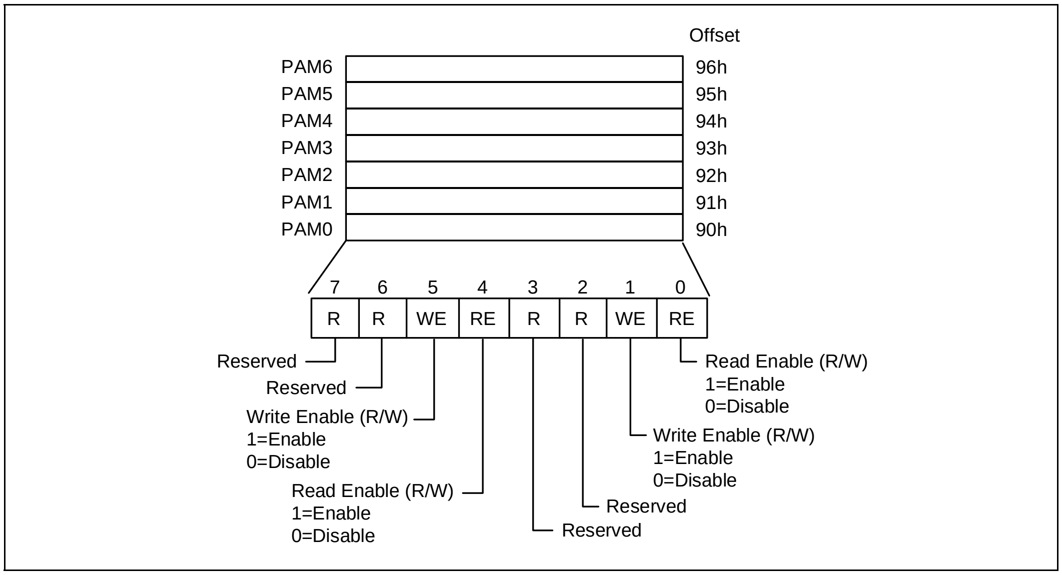


Table 6. PAM Register Attributes

PAM Reg	Attribute Bits				Memory Segment	Comments	Offset
PAM0[3:0]	Reserved				—	—	90h
PAM0[7:6]	Reserved				—	—	90h
PAM0[5:4]	R	R	WE	RE	0F0000h–0FFFFFh	BIOS Area	90h
PAM1[1:0]	R	R	WE	RE	0C0000h–0C3FFFh	ISA Add-on BIOS	91h
PAM1[7:4]	R	R	WE	RE	0C4000h–0C7FFFh	ISA Add-on BIOS	91h
PAM2[1:0]	R	R	WE	RE	0C8000h–0CBFFFh	ISA Add-on BIOS	92h
PAM2[7:4]	R	R	WE	RE	0CC000h–0CFFFFh	ISA Add-on BIOS	92h
PAM3[1:0]	R	R	WE	RE	0D0000h–0D3FFFh	ISA Add-on BIOS	93h
PAM3[7:4]	R	R	WE	RE	0D4000h–0D7FFFh	ISA Add-on BIOS	93h
PAM4[1:0]	R	R	WE	RE	0D8000h–0DBFFFh	ISA Add-on BIOS	94h
PAM4[7:4]	R	R	WE	RE	0DC000h–0DFFFFh	ISA Add-on BIOS	94h
PAM5[1:0]	R	R	WE	RE	0E0000h–0E3FFFh	BIOS Extension	95h
PAM5[7:4]	R	R	WE	RE	0E4000h–0E7FFFh	BIOS Extension	95h
PAM6[1:0]	R	R	WE	RE	0E8000h–0EBFFFh	BIOS Extension	96h
PAM6[7:4]	R	R	WE	RE	0EC000h–0EFFFFh	BIOS Extension	96h

For details on overall system address mapping scheme see Chapter 4.

DOS Application Area (00000h–9FFFh)

The DOS area is 640 KB in size and it is further divided into two parts. The 512-KB area at 0 to 7FFFFh is always mapped to the main memory controlled by the MCH, while the 128-KB address range from 080000 to 09FFFFh can be mapped to PCI_A or to main memory. By default this range is mapped to main memory and can be declared as a main memory hole (accesses forwarded to PCI_A) via the MCH FDHC configuration register.

Video Buffer Area (A0000h–BFFFFh)

Attribute bits do not control this 128-KB area. The host-initiated cycles in this region are always forwarded to either PCI_A unless this range is accessed in SMM mode. **Routing of accesses is controlled by the Legacy VGA control mechanism of the "virtual" PCI-to-PCI bridge device in the MCH.**

This area can be programmed as SMM area via the SMRAM register. When used as SMM space, this range cannot be accessed from the HI.

Expansion Area (C0000h–DFFFFh)

This 128-KB area is divided into eight, 16-KB segments, that can be assigned with different attributes via the PAM control register as defined by Table 6.

Extended System BIOS Area (E0000h–EFFFFh)

This 64-KB area is divided into four, 16-KB segments that can be assigned with different attributes via the PAM control register as defined by Table 6.

System BIOS Area (F0000h–FFFFFh)

This area is a single, 64-KB segment that can be assigned with different attributes via the PAM control register as defined by Table 6.

3.5.19 FDHC—Fixed Memory (ISA) Hole Control Register (Device 0)

Address Offset: 97h
Default Value: 00h
Access: R/W, RO
Size: 8 bits

This 8-bit register controls a fixed DRAM hole from 15 MB–16 MB.

Bit	Descriptions
7	**Hole Enable (HEN)—R/W.** This field enables a memory hole in DRAM space. The DRAM that lies "behind" this space is not remapped. 0 = Disable. No memory hole. 1 = Enable. Memory hole from 15 MB to 16 MB.
6:0	Reserved

3.5.20 SMRAM—System Management RAM Control Register (Device 0)

Address Offset: 9Dh
Default Value: 02h
Access: R/W, RO, Lock
Size: 8 bits

The SMRAMC register controls how accesses to Compatible and Extended SMRAM spaces are treated. The open, close, and lock bits function only when the G_SMRAME bit is set to 1. Also, the open bit must be reset before the lock bit is set.

Bit	Descriptions
7	Reserved
6	**SMM Space Open (D_OPEN)—R/W.** When D_OPEN=1 and D_LCK=0, the SMM space DRAM is made visible even when SMM decode is not active. This is intended to help BIOS initialize SMM space. Software should ensure that D_OPEN=1 and D_CLS=1 are not set at the same time.
5	**SMM Space Closed (D_CLS)—R/W.** When D_CLS = 1, SMM space DRAM is not accessible to data references, even if SMM decode is active. Code references may still access SMM space DRAM. This will allow SMM software to reference through SMM space to update the display, even when SMM is mapped over the VGA range. Software should ensure that D_OPEN=1 and D_CLS=1 are not set at the same time. Note that the D_CLS bit only applies to Compatible SMM space.
4	**SMM Space Locked (D_LCK)—R/W.** When D_LCK is set to 1, then D_OPEN is reset to 0 and D_LCK, D_OPEN, C_BASE_SEG, H_SMRAM_EN, TSEG_SZ and TSEG_EN become read only. D_LCK can be set to 1 via a normal configuration space write but can only be cleared by a Full Reset. The combination of D_LCK and D_OPEN provide convenience with security. The BIOS can use the D_OPEN function to initialize SMM space and then use D_LCK to “lock down” SMM space in the future so that no application software (or BIOS itself) can violate the integrity of SMM space, even if the program has knowledge of the D_OPEN function.
3	**Global SMRAM Enable (G_SMRARE)— R/W/L.** If set to 1, then Compatible SMRAM functions are enabled, providing 128 KB of DRAM accessible at the A0000h address while in SMM (ADS# with SMM decode). To enable Extended SMRAM function this bit has to be set to 1. Refer to the section on SMM for more details. Once D_LCK is set, this bit becomes read only.
2:0	**Compatible SMM Space Base Segment (C_BASE_SEG)—RO.** This field indicates the location of SMM space. SMM DRAM is not remapped. It is simply made visible if the conditions are right to access SMM space, otherwise the access is forwarded to HI. Since the MCH supports only the SMM space between A0000h and BFFFFh, this field is hardwired to 010.

3.5.21 ESMRAMC—Extended System Management RAM Control Register (Device 0)

Address Offset: 9Eh
Default Value: 38h
Access: R/W, R/WC, RO, Lock
Size: 8 bits

The Extended SMRAM register controls the configuration of Extended SMRAM space. The Extended SMRAM (E_SMRAM) memory provides a write-back cacheable SMRAM memory space that is above 1 MB.

Bit	Descriptions
7	**Enable High SMRAM (H_SMRAME)— R/W/L.** This bit controls the SMM memory space location (i.e., above 1 MB or below 1 MB). When G_SMRAME is 1 and H_SMRAME (this bit) is set to 1, the high SMRAM memory space is enabled. SMRAM accesses within the range 0FEDA0000h to 0FEDBFFFFh are remapped to DRAM addresses within the range 000A0000h to 000BFFFFh. Once D_LCK has been set, this bit becomes read only.
6	**Invalid SMRAM Access (E_SMERR)—R/WC.** This bit is set when the processor has accessed the defined memory ranges in Extended SMRAM (High Memory and T-segment) while not in SMM space and with the D-OPEN bit = 0. It is software's responsibility to clear this bit. **NOTE:** Software must write a 1 to this bit to clear it.
5	**SMRAM Cacheable (SM_CACHE)—RO.** Hardwired to 1.
4	**L1 Cache Enable for SMRAM (SM_L1)—RO.** Hardwired to 1.
3	**L2 Cache Enable for SMRAM (SM_L2)—RO.** Hardwired to 1.
2:1	**TSEG Size (TSEG_SZ)—R/W.** This field selects the size of the TSEG memory block if enabled. Memory from the top of DRAM space (TOUD +TSEG_SZ) to TOUD is partitioned away so that it may only be accessed by the processor interface and only then when the SMM bit is set in the request packet. Non-SMM accesses to this memory region are sent to the hub interface when the TSEG memory block is enabled. 00 =Reserved 01 =Reserved 10=(TOUD + 512 KB) to TOUD 11 =(TOUD + 1 MB) to TOUD
0	**TSEG Enable (T_EN)— R/W/L.** This bit is for enabling of SMRAM memory for Extended SMRAM space only. When G_SMRAME =1 and TSEG_EN = 1, the TSEG is enabled to appear in the appropriate physical address space. Note that once D_LCK is set, this bit becomes read only.

3.5.22 TOUD—Top of Used DRAM Register (Device 0)

Address Offset: C4–C5h
Default Value: 0400h
Access: RO, R/W
Size: 16 bits

Bit	Descriptions
15:3	**Top of Usable DRAM (TOUD)—R/W.** This register contains bits 31:19 of the maximum system memory address that is usable by the operating system. Address bits 31:19 imply a memory granularity of 512 KB. Configuration software should set this value to either the maximum amount of usable memory (minus tseg) in the system or to the minimum address allocated for PCI memory or the graphics aperture (minus tseg), whichever is smaller. Address bits 18:0 are assumed to be 0000h for the purposes of address comparison. This register must be set to at least 0400h for a minimum of 64 MB of system memory. To calculate the value of TOUD, configuration software should set this value to the **smaller** of the following tow cases: • **The maximum amount of usable memory in the system minus optional tseg.** • **The address allocated for PCI memory or the graphics aperture minus optional tseg.** **NOTE:** Even if the OS does not need any PCI space, TOUD should never be programmed above FEC0_0000h. If TOUD is programmed above this, address ranges that are reserved will become accessible to applications.
2:0	Reserved

3.5.23 MCHCFG—MCH Configuration Register (Device 0)

Address Offset: C6–C7h
Default Value: 0000h
Access: R/W, RO
Size: 16 bits

Bit	Descriptions
15:13	**Number of Stop Grant Cycles (NSG)—R/W.** This field represents the number of Stop Grant transactions expected on the FSB bus before a Stop Grant Acknowledge packet is sent to the ICH. This field is programmed by the BIOS after it has enumerated the processors and before it has enabled Stop Clock generation in the ICH. Once this field has been set, it should not be modified. Note that each enabled thread within each processor will generate Stop Grant Acknowledge transactions. 000 = HI Stop Grant sent after 1 FSB Stop Grant 001 = HI Stop Grant sent after 2 FSB Stop Grants 010–111= Reserved
12	Reserved
11:10	**System Memory Frequency Select (SMFREQ)—RW.** The reset value of these bits is 00. The DDR memory frequency is determined by the following table, and partly determined by the FSB frequency. FSBFREQ[1:0] =01SMFREQ[11:10]=01System Memory DDR set to 333 MHz FSBFREQ[1:0] =10SMFREQ[11:10]=01System Memory DDR set to 333 (320) MHz FSBFREQ[1:0] =10SMFREQ[11:10]=10System Memory DDR set to 400 MHz All other combinations are Intel Reserved Note that Memory I/O Clock always runs at 2X the frequency of the memory clock **NOTE:** When writing a new value to this register, software must perform a clock synchronization sequence to apply the new timings. The new value does not get applied until this is completed.
9:6	Reserved

Bit	Descriptions
5	Reserved
4	Reserved
3	Reserved
2	**FSB IOQ Depth (IOQD)—RO.** This bit is RO and reflects the HA7# strap value. It indicates the depth of the FSB IOQ. When the strap is sampled low, this bit will be a 0 and the FSB IOQ depth is set to 1. When the strap is sampled high, this bit will be a 1 and the FSB IOQ depth is set to the maximum (12 on the bus, 12 on the MCH). 0 = 1 deep 1 = 12 on the bus, 12 on the MCH
1:0	**FSB Frequency Select (FSBFREQ)—RO.** The default value of this bit is set by the strap assigned to the BSEL[1:0] pins and is latched at the rising edge of PWROK. 00 = Core Frequency is 100 MHz and the FSB frequency is 400 MHz 01 = Core Frequency is 133 MHz and the FSB frequency is 533 MHz 10 = Core Frequency is 200 MHz and the FSB frequency is 800 MHz 11 = Reserved

3.5.24 ERRSTS—Error Status Register (Device 0)

Address Offset: C8–C9h
Default Value: 0000h
Access: R/WC
Size: 16 bits

This register is used to report various error conditions via the SERR HI messaging mechanism. An SERR HI message is generated on a 0-to-1 transition of any of these flags (if enabled by the ERRCMD and PCICMD registers). These bits are set regardless of whether or not the SERR is enabled and generated.

Note: Software must write a 1 to clear bits that are set.

Bit	Descriptions
15:10	Intel Reserved
9	**Non-DRAM Lock Error (NDLOCK)—R/WC.** 0 = No Lock operation detected. 1 = MCH has detected a lock operation to memory space that did not map into DRAM. This bit is cleared when software writes a 1 to it.
8	**Software Generated SMI Flag—R/WC.** 0 = Source of an SMI was NOT the Device 2 Software SMI Trigger 1 = Source of an SMI was the Device 2 Software SMI Trigger.
7	**Multiple-bit DRAM ECC Error Flag (DMERR)—R/WC.** 0 = No non-correctable multiple-bit error for a memory read data transfer. 1 = If this bit is set to 1, a memory read data transfer had a non-correctable multiple-bit error. When this bit is set the address, channel number, and device number that caused the error are logged in the EAP register. Once this bit is set the EAP fields are locked until the processor clears this bit by writing a 1. Software uses bits [7,0] to detect whether the logged error address is for Single or Multiple-bit error. Once software completes the error processing, a value of 1 is written to this bit field to clear the value (back to 0) and unlock the error logging mechanism.
6	Reserved
5	**MCH Detects Unimplemented HI Special Cycle (HIAUSC)—R/WC.** 0 = No unimplemented Special Cycle on HI detected. 1 = MCH detects an Unimplemented Special Cycle on HI.

Bit	Descriptions
4	Reserved
3	Reserved
2	Reserved
1	Reserved
0	**Single-bit DRAM ECC Error Flag (DSERR)—R/WC.** 0 = No single-bit correctable DRAM ECC error detected for a memory read data transfer. 1 = A memory read data transfer had a single-bit correctable error and the corrected data was sent for the access. When this bit is set, the address, channel number, and device number that caused the error are logged in the EAP register. Once this bit is set, the EAP fields are locked to further single bit error updates until the processor clears this bit by writing a 1 to it. A multiple bit error that occurs after this bit is set will overwrite the EAP fields with the multiple bit error signature and the MEF bit will also be set. Software must write a 1 to clear this bit and unlock the error logging mechanism.

3.5.25 ERRCMD—Error Command Register (Device 0)

Address Offset: CA–CBh
Default Value: 0000h
Access: RO, R/W
Size: 16 bits

This register controls the MCH responses to various system errors. Since the MCH does not have a SERR# signal, SERR messages are passed from the MCH to the ICH over the hub interface. When a bit in this register is set, a SERR message will be generated on the hub interface when the corresponding flag is set in the ERRSTS register. The actual generation of the SERR message is globally enabled for Device 0 via the PCI Command register.

Bit	Descriptions
15:10	Intel Reserved
9	**SERR on Non-DRAM Lock (LCKERR)—R/W.** 0 = Disable 1 = Enable. The MCH will generate a HI SERR special cycle when a processor lock cycle is detected that does not hit system memory.
8	**SERR Multiple-Bit DRAM ECC Error (DMERR)—R/W.** 0 = Disable. 1 = Enable. The MCH generates a SERR message over HI when it detects a multiple-bit error reported by the DRAM controller. For systems not supporting ECC, this bit must be disabled.
7	**SERR on Single-bit ECC Error (DSERR)—R/W.** 0 = Disable. 1 = Enable. The MCH generates a SERR special cycle over HI when the DRAM controller detects a single bit error. For systems that do not support ECC this bit must be disabled.
6	**SERR on Target Abort on HI Exception (TAHLA)—R/W.** 0 = Disable. Reporting of this condition is disabled. 1 = Enable. MCH generates a SERR special cycle over HI when an MCH originated HI cycle is completed with a Target Abort completion packet or special cycle.
5	**SERR on Detecting HI Unimplemented Special Cycle (HIAUSCERR)—R/W.** 0 = Disable. MCH does not generate an SERR message for this event. SERR messaging for Device 0 is globally enabled in the PCICMD register. 1 = Enable. MCH generates a SERR message over HI when an Unimplemented Special Cycle is received on the HI.
4	Reserved

Bit	Descriptions
3	Reserved
2	Reserved
1	Reserved
0	Reserved

3.5.26 SMICMD—SMI Command Register (Device 0)

Address Offset: CC–CDh
Default Value: 0000h
Access: RO, R/W
Size: 16 bits

This register enables various errors to generate an SMI HI special cycle. When an error flag is set in the ERRSTS register, it can generate an SCI HI special cycle when enabled in the ERRCMD, SMICMD, or SCICMD registers, respectively. Note that one, and only one, message type can be enabled.

Bit	Descriptions
15:9	Reserved
8	**SMI on Multiple-Bit DRAM ECC Error—R/W.** 0 = Disable. 1 = Enable. The MCH generates an SMI HI message when it detects a multiple-bit error reported by the DRAM controller. For systems not supporting ECC, this bit must be disabled.
7	**SMI on Single-bit ECC Error—R/W.** 0 = Disable. 1 = Enable. The MCH generates an SMI HI special cycle when the DRAM controller detects a single-bit error. For systems that do not support ECC, this bit must be disabled.
6:0	Reserved

3.5.27 SCICMD—SCI Command Register (Device 0)

Address Offset: CE–CFh
Default Value: 0000h
Access: RO, R/W
Size: 16 bits

This register enables various errors to generate an SCI HI special cycle. When an error flag is set in the ERRSTS register, it can generate an SCI HI special cycle when enabled in the ERRCMD, SMICMD, or SCICMD registers, respectively. Note that one, and only one, message type can be enabled.

Bit	Descriptions
15:9	Reserved
8	**SCI on Multiple-Bit DRAM ECC Error—R/W.** 0 = Disable. 1 = Enable. The MCH generates an SCI HI message when it detects a multiple-bit error reported by the DRAM controller. For systems not supporting ECC, this bit must be disabled.
7	**SCI on Single-bit ECC Error—R/W.** 0 = Disable. 1 = Enable. The MCH generates an SCI HI special cycle when the DRAM controller detects a single bit error. For systems that do not support ECC, this bit must be disabled.
6:0	Reserved

3.5.28 SKPD—Scratchpad Data Register (Device 0)

Address Offset: DE–DFh
Default Value: 0000h
Access: R/W
Size: 16 bits

Bit	Descriptions
15:0	**Scratchpad (SCRTCH)—R/W.** These bits are R/W storage bits that have no effect on the MCH functionality.

3.5.29 CAPREG—Capability Identification Register (Device 0)

Address Offset: E4h–E9h
Default: 00000106A009h
Access: RO
Size 40 bits

The Capability Identification Register uniquely identifies chipset capabilities as defined in the following table.

Bit	Descriptions
47:28	Reserved
27:24	**CAPREG Version—RO.** This field has the value 0001b to identify the first revision of the CAPREG definition.
23:16	**Cap_length—RO.** This field has the value 06h indicating the structure length.
15:8	**Next_Pointer—RO.** This field has the value 00h signifying the end of the capabilities linked list.
7:0	**CAP_ID—RO.** This field has the value 09h to identify the CAP_ID assigned by the PCI SIG for Vendor Dependent CAP_PTR.

3.6 PCI-to-CSA Bridge Registers (Device 3)

This device is the virtual PCI-to-CSA bridge. This section contains the PCI configuration registers listed in order of ascending offset address.

Table 7. PCI-to-CSA Bridge Configuration Register Address Map (Device 3)

Address Offset	Register Symbol	Register Name	Default Value	Access
00–01h	VID3	Vendor Identification	8086h	RO
02–03h	DID3	Device Identification	257Bh	RO
04–05h	PCICMD3	PCI Command	0000h	RO,R/W
06–07h	PCISTS3	PCI Status	00A0h	RO,R/WC
08h	RID3	Revision Identification	see register description	RO
09	—	Reserved	—	—
0Ah	SUBC3	Sub-Class Code	04h	RO
0Bh	BCC3	Base Class Code	06h	RO
0Ch	—	Reserved	—	—
0Dh	MLT3	Master Latency Timer	00h	RO,R/W
0Eh	HDR3	Header Type	01h	RO
0F–17h	—	Reserved	—	—
18h	PBUSN3	Primary Bus Number	00h	R/W
19h	SBUSN3	Secondary Bus Number	00h	R/W
1Ah	SUBUSN3	Subordinate Bus Number	00h	R/W
1Bh	SMLT3	Secondary Bus Master Latency Timer	00h	RO,R/W
1Ch	IOBASE3	I/O Base Address	F0h	RO,R/W
1Dh	IOLIMIT3	I/O Limit Address	00h	RO,R/W
1E–1Fh	SSTS3	Secondary Status	02A0h	RO,R/WC
20–21h	MBASE3	Memory Base Address	FFF0h	RO,R/W
22–23h	MLIMIT3	Memory Limit Address	0000h	RO,R/W
24–25h	PMBASE3	Prefetchable Memory Base Limit Address	FFF0h	RO,R/W
26–27h	PMLIMIT3	Prefetchable Memory Limit Address	0000h	RO,R/W
28–3Dh	—	Reserved	—	—
3Eh	BCTRL3	Bridge Control	00h	RO,R/W
3Fh	—	Reserved	—	—
40h	ERRCMD3	Error Command	00h	RO,R/W
41–4Fh	—	Reserved	—	—
50–53h	CSACNTRL	CSA Control	0E04 2802h	RO,R/W
54–FFh	—	Reserved	—	—

3.6.1 VID3—Vendor Identification Register (Device 3)

Address Offset: 00h–01h
Default Value: 8086h
Access Attributes: RO
Size: 16 bits

The VID Register contains the vendor identification number. This 16-bit register, combined with the Device Identification Register, uniquely identify any PCI device.

Bit	Description
15:0	**Vendor Identification Number—RO.** This is a 16-bit value assigned to Intel.

3.6.2 DID3—Device Identification Register (Device 3)

Address Offset: 02h–03h
Default Value: 257Bh
Access Attributes: RO
Size: 16 bits

This 16-bit register, combined with the Vendor Identification register, uniquely identifies any PCI device.

Bit	Description
15:0	**Device Identification Number—RO.** This is a 16-bit value assigned to the MCH Device 3.

3.6.3 PCICMD3—PCI Command Register (Device 3)

Address Offset: 04h–05h
Default: 0000h
Access: RO, R/W
Size: 16 bits

Bit	Description
15:10	Reserved
9	**Fast Back-to-Back (FB2B)—RO.** Hardwired to 0.
8	**SERR# Enable (SERRE)—R/W.** This bit is a global enable bit for Device 3 SERR messaging. The MCH communicates the SERR# condition by sending a SERR message to the ICH. 0 = Disable. The SERR message is not generated by the MCH for Device 3. 1 = Enable. The MCH is enabled to generate SERR messages over the hub interface for specific Device 3 error conditions that are individually enabled in the BCTRL3 register. The error status is reported in the PCISTS3 register.
7	**Address/Data Stepping (ADSTEP)—RO.** Hardwired to 0.
6	**Parity Error Enable (PERRE)—RO.** Hardwired to 0. Parity checking is not supported on the primary side of this device.
5	Reserved
4	**Memory Write and Invalidate Enable (MWIE)—RO.** Hardwired to 0.
3	**Special Cycle Enable (SCE)—RO.** Hardwired to 0.

Bit	Description
2	**Bus Master Enable (BME)—R/W.** This bit is not functional. It is a R/W bit for compatibility with compliance testing software.
1	**Memory Access Enable (MAE)—R/W.** This bit must be set to 1 to enable the memory and pre-fetchable memory address ranges defined in the MBASE3, MLIMIT3, PMBASE3, and PMLIMIT3 registers. 0 = Disable (default). 1 = Enable.
0	**I/O Access Enable (IOAE)—R/W.** This bit must be set to 1 to enable the I/O address range defined in the IOBASE3 and IOLIMIT3 registers. 0 = Disable (default). 1 = Enable.

3.6.4 PCISTS3—PCI Status Register (Device 3)

Address Offset: 06h–07h
Default Value: 00A0h
Access: RO, R/WC
Size: 16 bits

PCISTS3 is a 16-bit status register that reports the occurrence of error conditions associated with primary side of the “virtual” PCI-to-CSA bridge in the MCH.

Bit	Description
15	**Detected Parity Error (DPE)—RO.** Hardwired to 0. Parity is not supported on the primary side of this device.
14	**Signaled System Error (SSE)—R/WC.** Software clears this bit by writing a 1 to it. 0 = No SERR message generated by Device 3 over HI. 1 = MCH Device 3 generated a SERR message over HI for an enabled Device 3 error condition. Device 3 error conditions are enabled in the ERRCMD, PCICMD3, and BCTRL3 registers. Device 3 error flags are read/reset from the ERRSTS and SSTS3 register.
13	**Received Master Abort Status (RMAS)—RO.** Hardwired to 0. The concept of a master abort does not exist on the primary side of this device.
12	**Received Target Abort Status (RTAS)—R/WC.** Hardwired to 0. The concept of a target abort does not exist on the primary side of this device.
11	**Signaled Target Abort Status (STAS)—RO.** Hardwired to 0. The concept of a target abort does not exist on primary side of this device.
10:9	**DEVSEL# Timing (DEVT)—RO.** Hardwired to 00b. MCH does not support subtractive decoding devices on bus 0. The value 00b indicates that Device 3 uses the fastest possible decode.
8	**Data Parity Detected (DPD)—R/WC.** Hardwired to 0. Since Parity Error Response is hardwired to disabled (and the MCH does not support any parity detection on the primary side of this device), this bit is hardwired to 0.
7	**Fast Back-to-Back (FB2B)—RO.** Hardwired to 1. The interface always supports fast back to back writes.
6	Reserved
5	**66/60 MHz PCI Capable (CAP66)—RO.** Hardwired to 1. CSA is 66 MHz capable.
4:0	Reserved

3.6.5 RID3—Revision Identification Register (Device 3)

Address Offset: 08h
Default Value: See following table
Access: RO
Size: 8 bits

This register contains the revision number of the MCH Device 3.

Bit	Description
7:0	**Revision Identification Number—RO.** This is an 8-bit value that indicates the revision identification number for the MCH Device 3. It is always the same as the value in RID. 02h = A-2 Stepping

3.6.6 SUBC3—Class Code Register (Device 3)

Address Offset: 0Ah
Default Value: 04h
Access: RO
Size: 8 bits

This register contains the Sub-Class Code for the MCH device 3.

Bit	Description
7:0	**Sub-Class Code (SUBC)—RO.** This is an 8-bit value that indicates the category of bridge into which the Device 3 of the MCH falls. 04h = PCI-to-PCI bridge.

3.6.7 BCC3—Base Class Code Register (Device 3)

Address Offset: 0Bh
Default Value: 06h
Access: RO
Size: 8 bits

This register contains the Base Class Code of the MCH Device 3.

Bit	Description
7:0	**Base Class Code (BASEC)—RO.** This is an 8-bit value that indicates the Base Class Code for the MCH Device 3. 06h = Bridge device.

3.6.8 MLT3—Master Latency Timer Register (Device 3)

Address Offset: 0Dh
Default Value: 00h
Access: RO, RW
Size: 8 bits

This functionality is not applicable. It is described here since these bits should be implemented as a read/write to prevent standard PCI-to-PCI bridge configuration software from getting "confused."

Bit	Description
7:3	**Scratchpad MLT (NA7:3)—R/W.** These bits return the value with which they are written; however, they have no internal function and are implemented as a scratchpad merely to avoid confusing software.
2:0	Reserved

3.6.9 HDR3—Header Type Register (Device 3)

Address Offset: 0Eh
Default Value: 01h
Access: RO
Size: 8 bits

This register identifies the header layout of the configuration space.

Bit	Description
7:0	**Header Type Register (HDR)—RO.** 01h = MCH Device 3 is a single function device with bridge header layout.

3.6.10 PBUSN3—Primary Bus Number Register (Device 3)

Address Offset: 18h
Default Value: 00h
Access: RO
Size: 8 bits

This register identifies that "virtual" PCI-to-PCI bridge is connected to bus 0.

Bit	Description
7:0	**Primary Bus Number (BUSN)—RO.** Configuration software typcially programs this field with the number of the bus on the primary side of the bridge. Since Device 3 is an internal device and its primary bus is always 0, these bits are read only and are hardwired to 00h.

3.6.11 SBUSN3—Secondary Bus Number Register (Device 3)

Address Offset: 19h
Default Value: 00h
Access: R/W
Size: 8 bits

This register identifies the bus number assigned to the second bus side of the "virtual" PCI-to-PCI bridge (i.e., to CSA). This number is programmed by the PCI configuration software to allow mapping of configuration cycles to CSA.

Bit	Description
7:0	**Secondary Bus Number (BUSN)—R/W.** This field is programmed by configuration software with the bus number assigned to CSA.

3.6.12 SMLT3—Secondary Bus Master Latency Timer Register (Device 3)

Address Offset: 1Bh
Default Value: 00h
Access: RO
Size: 8 bits.

Bit	Description
7:0	Reserved

3.6.13 IOBASE3—I/O Base Address Register (Device 3)

Address Offset: 1Ch
Default Value: F0h
Access: RO, R/W
Size: 8 bits

This register controls the processor-to-CSA I/O access routing based on the following formula:

$$IO\_BASE \le address \le IO\_LIMIT$$

Only the upper four bits are programmable. For the purpose of address decode, address bits A[11:0] are treated as 0. Thus, the bottom of the defined I/O address range will be aligned to a 4-KB boundary.

Bit	Description
7:4	**I/O Address Base (IOBASE)—R/W.** This field corresponds to A[15:12] of the I/O addresses passed by bridge 1 to CSA.
3:0	Reserved

3.6.14 IOLIMIT3—I/O Limit Address Register (Device 3)

Address Offset: 1Dh
Default Value: 00h
Access: RO, RW
Size: 8 bits

This register controls the processor-to-CSA I/O access routing based on the following formula:

$$IO\_BASE \leq address \leq IO\_LIMIT$$

Only the upper four bits are programmable. For the purpose of address decode, address bits A[11:0] are assumed to be FFFh. Thus, the top of the defined I/O address range will be at the top of a 4-KB aligned address block.

Bit	Description
7:4	**I/O Address Limit (IOLIMIT)—R/W.** This field corresponds to A[15:12] of the I/O address limit of Device 3. Devices between this upper limit and IOBASE3 will be passed to CSA.
3:0	Reserved

3.6.15 SSTS3—Secondary Status Register (Device 3)

Address Offset: 1E–1Fh
Default Value: 02A0h
Access: RO, RWC
Size: 16 bits

SSTS3 is a 16-bit status register that reports the occurrence of error conditions associated with the secondary side (i.e., CSA side) of the “virtual” PCI-to-PCI bridge in the MCH.

Note: For R/WC bits, software must write a 1 to clear bits that are set.

Bit	Description
15	**Detected Parity Error (DPE)— RO.** Hardwired to 0. Parity is not supported on the CSA interface.
14	**Received System Error (RSE)—R/WC.** 0 = No system error from the CSA device to the MCH. 1 = CSA device signals a system error to the MCH.
13	**Received Master Abort Status (RMAS)—R/WC.** 0 = No MCH master abort by the MCH to terminate a Host-to-CSA transfer. 1 = MCH terminated a Host-to-CSA transfer with an unexpected master abort.
12	**Received Target Abort Status (RTAS)—R/WC.** 0 = No target abort for MCH-initiated transaction on CSA. 1 = MCH-initiated transaction on CSA is terminated with a target abort.
11	**Signaled Target Abort Status (STAS)—RO.** Hardwired to 0. The MCH does not generate target abort on CSA.
10:9	**DEVSEL# Timing (DEVT)—RO.** Hardwired to 01b. This 2-bit field indicates the timing of the DEVSEL# signal when the MCH responds as a target on CSA. The value 01b (medium) indicates the time when a valid DEVSEL# can be sampled by initiator of the PCI cycle.
8	**Master Data Parity Detected (DPD)—RO.** Hardwired to 0. MCH does not implement GPERR# signal on CSA.
7	**Fast Back-to-Back (FB2B)—RO.** Hardwired to 1. MCH, as a target, supports fast back-to-back transactions on CSA.

Bit	Description
6	Reserved
5	**66/60 MHz PCI Capable (CAP66)—RO.** Hardwired to 1. CSA is 66 MHz capable.
4:0	Reserved

3.6.16 MBASE3—Memory Base Address Register (Device 3)

Address Offset: 20–21h
Default Value: FFF0h
Access: RO, RW
Size: 16 bits

This register controls the processor-to-CSA non-prefetchable memory access routing based on the following formula:

$$\text{MEMORY\_BASE} \leq \text{address} \leq \text{MEMORY\_LIMIT}$$

The Upper 12 bits of the register are read/write and correspond to the upper 12 address bits A[31:20] of the 32-bit address. The bottom four bits of this register are read only and return 0's when read. This register must be initialized by the configuration software. For the purpose of address decode, address bits A[19:0] are assumed to be 0. Thus, the bottom of the defined memory address range will be aligned to 1-MB boundary.

Bit	Description
15:4	**Memory Address Limit (MLIMIT)—R/W.** This field corresponds to A[31:20] of the lower limit of the memory range that will be passed by Device 3 bridge to CSA.
3:0	Reserved

3.6.17 MLIMIT3—Memory Limit Address Register (Device 3)

Address Offset: 22–23h
Default Value: 0000h
Access: RO, R/W
Size: 16 bits

This register controls the processor-to-CSA non-prefetchable memory access routing based on the following formula:

$$\text{MEMORY\_BASE} \leq \text{address} \leq \text{MEMORY\_LIMIT}$$

The upper 12 bits of the register are read/write and correspond to the upper 12 address bits A[31:20] of the 32-bit address. The bottom four bits of this register are read only and return 0's when read. This register must be initialized by the configuration software. For the purpose of address decode, address bits A[19:0] are assumed to be FFFFFh. Thus, the top of the defined memory address range will be at the top of a 1-MB aligned memory block.

Note: Memory ranges covered by MBASE and MLIMIT registers are used to map non-prefetchable CSA address ranges (typically, where control/status memory-mapped I/O data structures of the graphics controller will reside) and PMBASE and PMLIMIT are used to map prefetchable address ranges (typically, graphics local memory). This segregation allows application of USWC space attribute to be performed in a true plug-and-play manner to the prefetchable address range for improved processor-CSA memory access performance.

Note: Configuration software is responsible for programming all address range registers (prefetchable, non-prefetchable) with the values that provide exclusive address ranges (i.e., prevent overlap with each other and/or with the ranges covered with the main memory). There is no provision in the MCH hardware to enforce prevention of overlap and operations of the system in the case of overlap are not guaranteed.

Bit	Description
15:4	**Memory Address Limit (MLIMIT)—R/W.** This field corresponds to A[31:20] of the memory address that corresponds to the upper limit of the range of memory accesses that will be passed by the Device 3 bridge to CSA.
3:0	Reserved

3.6.18 PMBASE3—Prefetchable Memory Base Address Register (Device 3)

Address Offset: 24–25h
Default Value: FFF0h
Access: R/W, RO
Size: 16 bits

This register controls the processor-to-CSA prefetchable memory access routing based on the following formula:

PREFETCHABLE_MEMORY_BASE ≤ address ≤ PREFETCHABLE_MEMORY_LIMIT

The upper 12 bits of the register are read/write and correspond to the upper 12 address bits A[31:20] of the 32-bit address. The bottom four bits of this register are read only and return 0's when read. This register must be initialized by the configuration software. For the purpose of address decode, address bits A[19:0] are assumed to be 0. Thus, the bottom of the defined memory address range will be aligned to a 1-MB boundary.

Bit	Description
15:4	**Prefetchable Memory Address Base (PMBASE)—R/W.** This field corresponds to A[31:20] of the lower limit of the address range passed by bridge Device 3 across CSA.
3:0	Reserved

3.6.19 PMLIMIT3—Prefetchable Memory Limit Address Register (Device 3)

Address Offset: 26–27h
Default Value: 0000h
Access: R/W, RO
Size: 16 bits

This register controls the processor-to-CSA prefetchable memory access routing based on the following formula:

PREFETCHABLE_MEMORY_BASE ≤ address ≤ PREFETCHABLE_MEMORY_LIMIT

The upper 12 bits of the register are read/write and correspond to the upper 12 address bits A[31:20] of the 32-bit address. The bottom 4 bits of this register are read only and return 0's when read. This register must be initialized by the configuration software. For the purpose of address decode, address bits A[19:0] are assumed to be FFFFFh. Thus, the top of the defined memory address range will be at the top of a 1-MB aligned memory block. Note that the prefetchable memory range is supported to allow segregation by the configuration software between the memory ranges that must be defined as UC and the ones that can be designated as a USWC (i.e., prefetchable) from the processor perspective.

Bit	Description
15:4	**Prefetchable Memory Address Limit (PMLIMIT)—R/W.** This field corresponds to A[31:20] of the upper limit of the address range passed by bridge Device 3 across CSA.
3:0	Reserved

3.6.20 BCTRL3—Bridge Control Register (Device 3)

Address Offset: 3Eh
Default Value: 00h
Access: R/W, RO
Size: 8 bits

Bit	Description
7	**Fast Back-to-Back Enable (FB2BEN)—RO.** Hardwired to 0. The MCH does not generate fast back-to-back cycles as a master on AGP.
6	**Secondary Bus reset (SREST)—RO.** Hardwired to 0. The MCH does not support the generation of reset via this bit on the AGP.
5	**Master Abort Mode (MAMODE)—RO.** Hardwired to 0. This means that, when acting as a master on CSA, the MCH will discard writes and return all 1's during reads when a master abort occurs.
4	Reserved
3	**VGA Enable (VGAEN)—R/W.** This bit controls the routing of processor-initiated transactions targeting VGA compatible I/O and memory address ranges. This bit works in conjunction with the MCHCFG[MDAP] bit (Device 0, offset C6h) as described in Table 8.
2	**ISA Enable (ISAEN)—R/W.** This bit modifies the response by the MCH to an I/O access issued by the processor that targets ISA I/O addresses. This applies only to I/O addresses that are enabled by the IOBASE and IOLIMIT registers. 0 = Disable (default). All addresses defined by the IOBASE and IOLIMIT for processor I/O transactions will be mapped to CSA. 1 = Enable. The MCH will not forward to CSA any I/O transactions addressing the last 768 bytes in each 1-KB block, even if the addresses are within the range defined by the IOBASE and IOLIMIT registers. Instead of going to CSA, these cycles will be forwarded to the hub interface where they can be subtractively or positively claimed by the ISA bridge.
1	**SERR Enable (SERREN)—RO.** Hardwired to 0. This bit normally controls forwarding SERR# on the secondary interface to the primary interface. The MCH does not support the SERR# signal on the CSA bus.
0	**Parity Error Response Enable (PEREN)—RO.** Hardwired to 0

Table 8. VGAEN and MDAP Definitions

VGAEN	MDAP	Description
0	0	All References to MDA and VGA space are routed to HI.
0	1	Illegal combination.
1	0	All VGA references are routed to this bus. MDA references are routed to HI.
1	1	All VGA references are routed to this bus. MDA references are routed to HI.

3.6.21 ERRCMD3—Error Command Register (Device 3)

Address Offset: 40h
Default Value: 00h
Access: R/W, RO
Size: 8 bits

Bit	Description
7:1	Reserved
0	**SERR on Receiving Target Abort (SERTA)—R/W.** 0 = The MCH does not assert a SERR message upon receipt of a target abort on CSA. 1 = The MCH generates a SERR message over CSA upon receiving a target abort on CSA. SERR messaging for Device 3 is globally enabled in the PCICMD3 register.

3.6.22 CSACNTRL—CSA Control Register (Device 3)

Address Offset: 50–53h
Default Value: 0E042802h
Access: R/W, RO
Size: 32 bits

Bit	Description
31:29	**First Subordinate CSA (CSA_SUB_FIRST)—R/W.** This field stores the lowest subordinate CI hub number.
28	Reserved
27:25	**Last Subordinate CSA (CSA_SUB_LAST)—R/W.** This field stores the highest subordinate CSA hub number.
24:16	Reserved
15:14	**CSA Width (CSA_WIDTH)—R/W.** This field describes the used width of the data bus. 00 = 8 bit 01 = Reserved 10 = Reserved 11 = Reserved
13:0	Intel Reserved

3.7 Overflow Configuration Registers (Device 6)

Device 6 is the Overflow Device for Device 0. The registers in this section are arranged in ascending order of the address offset. Table 9 provides the configuration register address map.

Table 9. Overflow Device Configuration Register Address Map (Device 6)

Address Offset	Register Symbol	Register Name	Default Value	Access
00–01h	VID6	Vendor Identification	8086h	RO
02–03h	DID6	Device Identification	257Eh	RO
04–05h	PCICMD6	PCI Command Register	0000h	RO, R/W
06–07h	PCISTS6	PCI Status Register	0080h	RO
08h	RID6	Revision Identification	see register description	RO
09h	—	Reserved	—	—
0Ah	SUBC6	Sub-Class Code	80h	RO
0Bh	BCC6	Base Class Code	08h	RO
0Ch–0Dh	—	Reserved	—	—
0Eh	HDR6	Header Type	00h	RO
0Fh	—	Reserved	—	—
10–13h	BAR6	Base Address	00000000h	RO
14–2Bh	—	Reserved	—	—
2C–2Dh	SVID6	Subsystem Vendor Identification	0000h	R/WO
2E–2Fh	SID6	Subsystem Identification	0000h	R/WO
30–3Fh	—	Reserved	—	—
40–FFh	—	Intel Reserved	—	—

3.7.1 VID6—Vendor Identification Register (Device 6)

Address Offset: 00–01h
Default Value: 8086h
Access: RO
Size: 16 bits

The VID Register contains the vendor identification number. This 16-bit register, combined with the Device Identification Register, uniquely identifies any PCI device.

Bit	Descriptions
15:0	**Vendor Identification (VID)—RO.** This register field contains the PCI standard identification for Intel.

3.7.2 DID6—Device Identification Register (Device 6)

Address Offset: 02–03h
Default Value: 257Eh
Access: RO
Size: 16 bits

This 16-bit register, combined with the Vendor Identification register, uniquely identifies any PCI device.

Bit	Descriptions
15:0	**Device Identification Number (DID)—RO.** This is a 16-bit value assigned to the MCH Host-HI bridge Function 0.

3.7.3 PCICMD6—PCI Command Register (Device 6)

Address Offset: 04–05h
Default Value: 0000h
Access: RO, R/W
Size: 16 bits

Since MCH Device 0 does not physically reside on PCI_A, many of the bits are not implemented.

Bit	Descriptions
15:10	Reserved
9	**Fast Back-to-Back Enable (FB2B)—RO.** Hardwired to 0.
8	**SERR Enable (SERRE)—RO.** Hardwired to 0.
7	**Address/Data Stepping Enable (ADSTEP)—RO.** Hardwired to 0.
6	**Parity Error Enable (PERRE)—RO.** Hardwired to 0.
5	**VGA Palette Snoop Enable (VGASNOOP)—RO.** Hardwired to 0.
4	**Memory Write and Invalidate Enable (MWIE)—RO.** Hardwired to 0.
3	**Special Cycle Enable (SCE)—RO.** Hardwired to 0.
2	**Bus Master Enable (BME)—RO.** Hardwired to 0.
1	**Memory Access Enable (MAE)—R/W.** Set this bit to 1 to enable Device 6 memory space accesses. 0 = Disable (default). 1 = Enable.
0	**I/O Access Enable (IOAE)—R/W.** This bit must be set to 1 to enable the I/O address range defined in the IOBASE3 and IOLIMIT3 registers. 0 = Disable (default). 1 = Enable.

3.7.4 PCISTS6—PCI Status Register (Device 6)

Address Offset: 06–07h
Default Value: 0080h
Access: RO
Size: 16 bits

PCISTS6 is a 16-bit status register that reports the occurrence of error events on Device 6, Function 0's PCI interface. Since MCH Device 6 does not physically reside on PCI_0, many of the bits are not implemented.

Bit	Descriptions
15	**Detected Parity Error (DPE)—RO.** Hardwired to 0.
14	**Signaled System Error (SSE)—RO.** Hardwired to 0.
13	**Received Master Abort Status (RMAS)—RO.** Hardwired to 0.
12	**Received Target Abort Status (RTAS)—RO.** Hardwired to 0.
11	**Signaled Target Abort Status (STAS)—RO.** Hardwired to 0.
10:9	**DEVSEL Timing (DEVT)—RO.** Hardwired to 00. Device 6 does not physically connect to PCI_A. These bits are set to 00 (fast decode) so that optimum DEVSEL timing for PCI_A is not limited by the MCH.
8	**Master Data Parity Error Detected (DPD)—RO.** Hardwired to 0.
7	**Fast Back-to-Back (FB2B)—RO.** Hardwired to 1. This bit is set to 1 (indicating fast back-to-back capability) so that the optimum setting for PCI_A is not limited by the MCH.
6:0	Reserved

3.7.5 RID6—Revision Identification Register (Device 6)

Address Offset: 08h
Default Value: See following table
Access: RO
Size: 8 bits

This register contains the revision number of the MCH Device 0.

Bit	Descriptions
7:0	**Revision Identification Number (RID)—RO.** This is an 8-bit value that indicates the revision identification number for the MCH Device 6. 02h = A-2 Stepping

3.7.6 SUBC6—Sub-Class Code Register (Device 6)

Address Offset: 0Ah
Default Value: 80h
Access: RO
Size: 8 bits

This register contains the Sub-Class Code for the MCH Device 0.

Bit	Descriptions
7:0	**Sub-Class Code (SUBC)—RO.** This is an 8-bit value that indicates the category of device for the MCH Device 6. 80h = Other system peripheral.

3.7.7 BCC6—Base Class Code Register (Device 6)

Address Offset: 0Bh
Default Value: 08h
Access: RO
Size: 8 bits

This register contains the Base Class Code for the MCH Device 0.

Bit	Descriptions
7:0	**Base Class Code (BASEC)—RO.** This is an 8-bit value that indicates the category of Device for the MCH Device 6. 08h = Other system peripherals.

3.7.8 HDR6—Header Type Register (Device 6)

Address Offset: 0Eh
Default Value: 00h
Access: RO
Size: 8 bits

This register identifies the header layout of the configuration space.

Bit	Descriptions
7:0	**PCI Header (HDR)—RO.** 00h = Single function device with standard header layout.

3.7.9 BAR6—Memory Delays Base Address Register (Device 6)

Address Offset: 10–13h
Default Value: 00000000h
Access: RO, R/W
Size: 32 bits

This register is a standard PCI scheme to claim a memory-mapped address range. This memory-mapped address range can be enabled once the relevant enable bit in the PCI command register is set to 1.

Bit	Descriptions
31:12	**Memory base Address—R/W.** Set by the OS, these bits correspond to address signals [31:13].
11:4	**Address Mask—RO.** Hardwired to 00h to indicate 4-KB address range. This reserves 4 KB of memory-mapped address space.
3	**Prefetchable—RO.** This bit indicates the prefetchability of the requested memory address range. 0 = Not prefetchable. The memory range is not prefetchable and may have read side effects. 1 = Prefetchable. The memory address range is prefetchable (i.e., has no read side effects and returns all bytes on reads regardless of byte enables) and byte merging of write transactions is allowed.
2:1	**Memory Type (TYPE)—RO.** Hardwired to 00 to indicate that the address range defined by the upper bits of this register can be located anywhere in the 32-bit address space as per the PCI specification for base address registers.
0	**Memory Space Indicator (MSPACE)—RO.** Hardwired to 0 to identify memory space.

3.7.10 SVID6—Subsystem Vendor Identification Register (Device 6)

Address Offset: 2C–2Dh
Default Value: 0000h
Access: R/WO
Size: 16 bits

This value is used to identify the vendor of the subsystem.

Bit	Descriptions
15:0	**Subsystem Vendor ID (SUBVID)—R/WO.** This field should be programmed during boot-up to indicate the vendor of the system board. After it has been written once, it becomes read only.

3.7.11 SID6—Subsystem Identification Register (Device 6)

Address Offset: 2E–2Fh
Default Value: 0000h
Access: R/WO
Size: 16 bits

This value is used to identify a particular subsystem.

Bit	Descriptions
15:0	**Subsystem ID (SUBID)—R/WO.** This field should be programmed during BIOS initialization. After it has been written once, it becomes read only.

3.8 Device 6 Memory-Mapped I/O Register Space

The DRAM timing and delay registers are located in the memory-mapped register (MMR) space of Device 6. Table 10 provides the register address map for this set of registers.

Note: All accesses to these memory-mapped registers must be made as a single DWord (4 bytes) or less. Access must be aligned on a natural boundary.

Table 10. Device 6 Memory-Mapped I/O Register Address Map

Address Offset	Register Symbol	Register Name	Default Value	Access
0000h	DRB0	DRAM Row 0 Boundary	01h	RO, RW
0001h	DRB1	DRAM Row 1 Boundary	01h	RO, RW
0002h	DRB2	DRAM Row 2 Boundary	01h	RO, RW
0003h	DRB3	DRAM Row 3 Boundary	01h	RO, RW
0004h	DRB4	DRAM Row 4 Boundary	01h	RO, RW
0005h	DRB5	DRAM Row 5 Boundary	01h	RO, RW
0006h	DRB6	DRAM Row 6 Boundary	01h	RO, RW
0007h	DRB7	DRAM Row 7 Boundary	01h	RO, RW
0008–000Bh	—	Intel Reserved	—	—

Table 10. Device 6 Memory-Mapped I/O Register Address Map (Continued)

Address Offset	Register Symbol	Register Name	Default Value	Access
0010h	DRA0,1	DRAM Row 0,1 Attribute	00h	RO, RW
0011h	DRA2,3	DRAM Row 2,3 Attribute	00h	RO, RW
0012h	DRA4,5	DRAM Row 4,5 Attribute	00h	RO, RW
0013h	DRA6,7	DRAM Row 6,7 Attribute	00h	RO, RW
0014–005Fh	—	Intel Reserved	—	—
0060–0063h	DRT	DRAM Timing	0000 0000h	RW
0064–0067h	—	Intel Reserved	—	—
0068–006Bh	DRC	DRAM Controller Mode	0001 0001h	RW, RO
006C–FFFFh	—	Intel Reserved	—	—

3.8.1 DRB[0:7]—DRAM Row Boundary Registers (Device 6, MMR)

Address Offset: 0000h–0007h (DRB0–DRB7)
Default Value: 00h
Access: RO, R/W
Size: 8 bits each register

The DRAM row Boundary registers define the upper boundary address of each DRAM row. Each row has its own single-byte DRB register. The granularity of these registers is 64 MB. For example, a value of 1 in DRB0 indicates that 64 MB of DRAM has been populated in the first row. When in either of the two dual-channel modes, the granularity of these registers is still 64 MB. In this case, the lowest order bit in each register is always programmed to 0 yielding a minimum granularity of 128 MB. Bit 7 of each of these registers is reserved and must be programmed to 0. The remaining 7 bits of each of these registers are compared against address lines 31:26 to determine which row is being addressed by the current cycle. In either of the dual-channel modes, the MCH supports a total of 4 rows of memory (only DRB0-3 are used). When in either of the dual-channel modes and four rows populated with 512-Mb technology, x8 devices, the largest memory size of 4 GB is supported. In this case, DRB3 is programmed to 40h. In the dual channel modes, DRB[7:4] must be programmed to the same value as DRB3. When in single-channel mode, all eight DRB registers are used. In this case, DRB[3:0] are used for the rows in channel A and DRB[7:4] are used for rows populated in channel B. If only channel A is populated, then only DRB[3:0] are used. DRB[7:4] are programmed to the same value as DBR3. If only channel B is populated, then DRB[7:4] are used and DRB[3:0] are programmed to 00h. When both channels are populated but not identically, then all of the DRB registers are used. This configuration is referred to as “virtual single-channel mode.”

Row0: 0000h
Row1: 0001h
Row2: 0002h
Row3: 0003h
Row4: 0004h
Row5: 0005h
Row6: 0006h
Row7: 0007h
0008h, reserved
0009h, reserved
000Ah, reserved
000Bh, reserved

000Ch, reserved
000Dh, reserved
000Eh, reserved
000Fh, reserved

DRB0 = Total memory in Row0 (in 64-MB increments)
DRB1 = Total memory in Row0 + Row1 (in 64-MB increments)
DRB2 = Total memory in Row0 + Row1 + Row2 (in 64-MB increments)
DRB3 = Total memory in Row0 + Row1 + Row2 + Row3 (in 64-MB increments)
DRB4 = Total memory in Row0 + Row1 + Row2 + Row3 + Row4 (in 64-MB increments)
DRB5 = Total memory in Row0 + Row1 + Row2 + Row3 + Row4 + Row5 (in 64-MB increments)
DRB6 = Total memory in Row0 + Row1 + Row2 + Row3 + Row4 + Row5 + Row6 (in 64-MB increments)
DRB7 = Total memory in Row0 + Row1 + Row2 + Row3 + Row4 + Row5 + Row6 + Row7 (in 64-MB increments)

Each row is represented by a byte. Each byte has the following format.

Bit	Description
7	Reserved
6:0	**DRAM Row Boundary Address—R/W.** This 7-bit value defines the upper and lower addresses for each DRAM row. This 7-bit value is compared against address lines 0, 31:26 (0 is concatenated with the address bits 31:26) to determine which row the incoming address is directed. Default= 0000001b

3.8.2 DRA— DRAM Row Attribute Register (Device 6, MMR)

Address Offset: 0010h—0013h
Default Value: 00h
Access: RO, R/W
Size: 8 bits each register

The DRAM Row Attribute registers define the page sizes to be used when accessing different rows or pairs of rows. The minimum page size of 4 KB occurs when in single-channel mode and either 128-Mb, x16 devices are populated or 256-Mb, x16 devices are populated. The maximum page size of 32 KB occurs when in dual-channel mode and 512 MB, x8 devices are populated. Each nibble of information in the DRA registers describes the page size of a row or pair of rows: When in either of the dual-channel modes, only registers 10h and 11h are used. The page size programmed reflects the page size for the pair of DIMMS installed. When in single-channel mode, registers 10h and 11h are used to specify page sizes for channel A and registers 12h and 13h are used to specify page sizes for channel B. **If the associated row is not populated, the field must be left at the default value.**

Row0, 1: 0010h
Row2, 3: 0011h
Row4, 5: 0012h
Row6, 7: 0013h

7	6 4	3	2 0
Rsvd	Row Attribute for Row 1	Rsvd	Row Attribute for Row 0

7	6 4	3	2 0
Rsvd	Row Attribute for Row 3	Rsvd	Row Attribute for Row 2

7	6 4	3	2 0
Rsvd	Row Attribute for Row 5	Rsvd	Row Attribute for Row 4

7	6 4	3	2 0
Rsvd	Row Attribute for Row 7	Rsvd	Row Attribute for Row 6

Bit	Description
7	Reserved
6:4	**Row Attribute for Odd-Numbered Row—R/W.** This field defines the page size of the corresponding row. If the associated row is not populated, this field must be left at the default value. 000 = 4 KB 001 = 8 KB 010 = 16 KB 011 = 32 KB Others = Reserved
3	Reserved
2:0	**Row Attribute for Even-Numbered Row—R/W.** This field defines the page size of the corresponding row. If the associated row is not populated, this field must be left at the default value. 000 = 4 KB 001 = 8 KB 010 = 16 KB 011 = 32 KB Others = Reserved

3.8.3 DRT—DRAM Timing Register (Device 6, MMR)

Address Offset: 0060h—0063h
Default Value: 00000000h
Access: R/W
Size: 32 bits

This register controls the timing of micro-commands. When in virtual single-channel mode, the timing fields specified here apply even if two back-to-back cycles are to different physical channels. That is, the controller acts as if the two cycles are to the same physical channel.

Bit	Description
31:11	Intel Reserved
10	**Activate to Precharge delay (t_{RAS}), Max—R/W.** These bits control the number of DRAM clocks for t_{RAS} maximum. 0 = 120 µs 1 = 70 µs **NOTE:** DDR333 DRAM requires a shorter T_{RAS} (max) of 70 µs

Bit	Description
9:7	**Activate to Precharge delay (t_{RAS}), Min—R/W.** These bits control the number of DRAM clocks for t_{RAS} minimum. 000 = 10 DRAM clocks 001 = 9 DRAM clocks 010 = 8 DRAM clocks 011 = 7 DRAM clocks 100 = 6 DRAM clocks 101 = 5 DRAM clocks others = Reserved
6:5	**CAS# Latency (t_{CL})—R/W.** 00 = 2.5 DRAM clocks 01 = 2 DRAM clocks 10 = 3 DRAM clocks 11 = Reserved
4	Intel Reserved
3:2	**DRAM RAS# to CAS# Delay (t_{RCD})—R/W.** This bit controls the number of clocks inserted between an active command and a read or write command to that bank. 00 = 4 DRAM clocks 01 = 3 DRAM clocks 10 = 2 DRAM clocks 11 = Reserved
1:0	**DRAM RAS# Precharge (t_{RP})—R/W.** This bit controls the number of clocks that are inserted between a precharge command and an active command to the same bank. 00 = 4 DRAM clocks (DDR333) 01 = 3 DRAM clocks 10 = 2 DRAM clocks 11 = Reserved

3.8.4 DRC—DRAM Controller Mode Register (Device 6, MMR)

Address Offset: 0068h—006Bh
Default Value: 00000001h
Access: R/W, RO
Size: 32 bits

Bit	Description
31:30	Reserved
29	**Initialization Complete (IC)—R/W.** This bit is used for communication of the software state between the memory controller and the BIOS. 1 = BIOS sets this bit to 1 after initialization of the DRAM memory array is complete.
28	Reserved
27:23	Intel Reserved
22:21	**Number of Channels (CHAN)—RO.** This field reflects that the MCH controller supports two modes of operation. 00 = Single-channel or virtual single-channel 01 = Dual-channel 10 = Reserved 11 = Reserved

Bit	Description
20	Reserved
19:18	**DRAM Data Integrity Mode (DDIM)—R/W.** These bits select data integrity mode. 00 = Non-ECC mode 01 = ECC enabled Other = Reserved
17:11	Reserved
10:8	**Refresh Mode Select (RMS)—R/W.** This field determines whether refresh is enabled and, if so, at what rate refreshes will be executed. 000 = Reserved 001 = Refresh enabled. Refresh interval is 15.6 µsec 010 = Refresh enabled. Refresh interval is 7.8 µsec 011 = Refresh enabled. Refresh interval is 64 µsec 111 = Refresh enabled. Refresh interval is 64 clocks (fast refresh mode) Other = Reserved
7	Reserved
6:4	**Mode Select (SMS)—R/W.** These bits select the special operational mode of the DRAM interface. The special modes are intended for initialization at power up. Note that FCSEN (fast CS#) must be set to 0 while SMS cycles are performed. It is expected that BIOS may program FCSEN to possible 1 only after initialization. 000 =Post Reset state – When the MCH exits reset (power-up or otherwise), the mode select field is cleared to 000. During any reset sequence, while power is applied and reset is active, the MCH de-asserts all CKE signals. After internal reset is de-asserted, CKE signals remain de-asserted until this field is written to a value different than 000. On this event, all CKE signals are asserted. During suspend (S3, S4), the MCH internal signal triggers the DRAM controller to flush pending commands and enter all rows into Self-Refresh mode. As part of the resume sequence, the MCH will be reset, which will clear this bit field to 000 and maintain CKE signals de-asserted. After internal reset is de-asserted, CKE signals remain de-asserted until this field is written to a value different than 000. On this event, all CKE signals are asserted. 001 =NOP Command Enable – All processor cycles to DRAM result in a NOP command on the DRAM interface. 010 =All Banks Pre-charge Enable – All processor cycles to DRAM result in an “all banks precharge” command on the DRAM interface. 011 =Mode Register Set Enable – All processor cycles to DRAM result in a “mode register” set command on the DRAM interface. Host address lines are mapped to DRAM address lines to specify the command sent. Host address HA[13:3] are mapped to memory address SMA[5:1]. 100 =Extended Mode Register Set Enable – All processor cycles to DRAM result in an “extended mode register set” command on the DRAM interface. Host address lines are mapped to DRAM address lines to specify the command sent. Host address lines are mapped to DRAM address lines to specify the command sent. Host address HA[13:3] are mapped to memory address SMA[5:1]. 101 =Reserved 110 =CBR Refresh Enable – In this mode all processor cycles to DRAM result in a CBR cycle on the DRAM interface 111 =Normal operation
3:2	Intel Reserved
1:0	**DRAM Type (DT)—RO.** This field is used to select between supported DRAM types. 00 = Reserved 01 = Dual data rate DRAM Other = Reserved

§

System Address Map 4

The processor used in a Intel E7210 chipset-based system supports 4 GB of addressable memory space and 64 KB+3 of addressable I/O space. There is a programmable memory address space under the 1 MB region that is divided into regions that can be individually controlled with programmable attributes (e.g., disable, read/write, write only, or read only). Attribute programming is described in the Chapter 3. This section focuses on how the memory space is partitioned and the use of the separate memory regions.

The next Pentium 4 processor, code named Prescott, supports addressing of memory ranges larger than 4 GB. The MCH claims any processor access over 4 GB and terminates the transaction without forwarding it to the hub interface. For reads, the MCH returns all 0’s on the host bus. Note that the Intel E7210 chipset platform does not support the PCI Dual Address Cycle Mechanism and, therefore, does not allow addressing of greater than 4 GB on the hub interface.

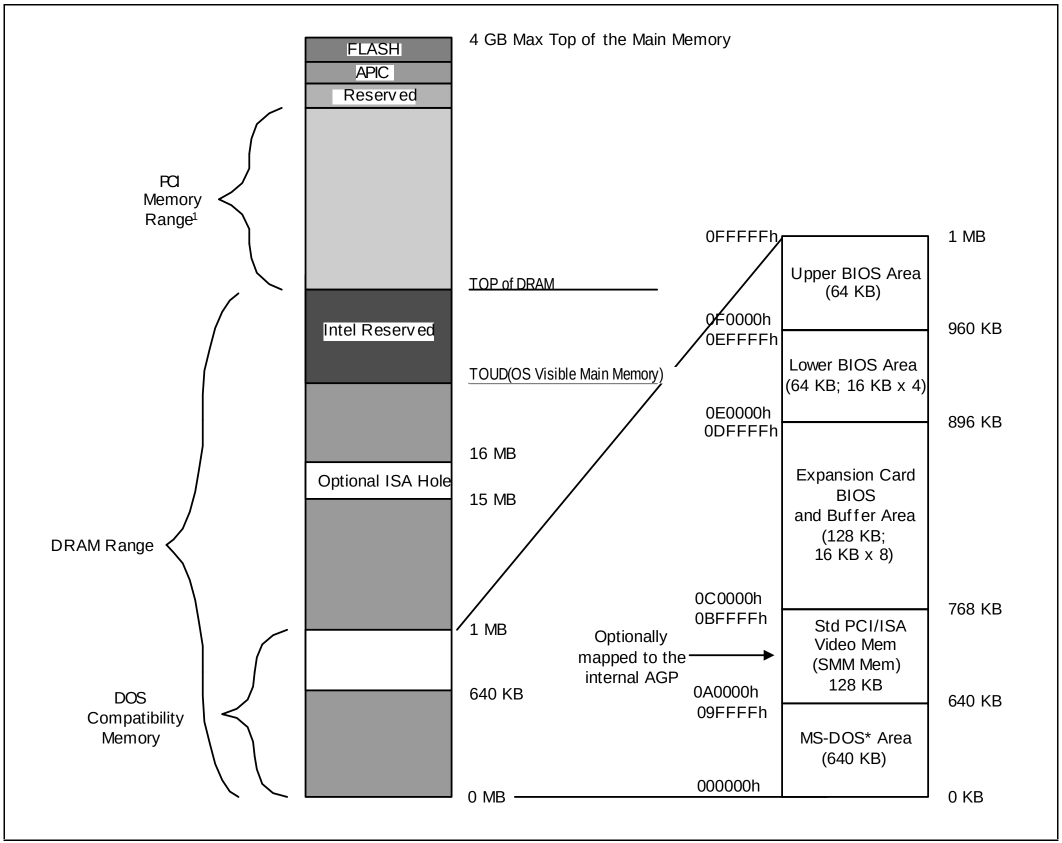
The Intel E7210 chipset memory map includes a number of programmable ranges.

Note: All of these ranges must be unique and non-overlapping. There are no hardware interlocks to prevent problems in the case of overlapping ranges. Accesses to overlapped ranges may produce indeterminate results.

4.1 System Memory Address Ranges

The MCH provides a maximum system memory address decode space of 4 GB. The MCH does not remap APIC memory space. The MCH does not limit system memory space in hardware. **It is the BIOS or system designers responsibility to limit memory population so that adequate PCI, High BIOS, and APIC memory space can be allocated.** Figure 7 provides details on mapping specific memory regions as defined and supported by the MCH.

Figure 7. Detailed Memory System Address Map



NOTE: Contains PCI, and ICH ranges.

4.2 Compatibility Area

This area is divided into the following address regions:

- 0–640 KB MS-DOS Area.
- 640–768 KB Video Buffer Area.
- 768–896 KB in 16-KB sections (total of eight sections) - Expansion Area.
- 896 -960 KB in 16-KB sections (total of four sections) - Extended System BIOS Area.
- 960-KB–1-MB memory (BIOS Area) - System BIOS Area.

There are fifteen memory segments in the compatibility area (see Table 11). Thirteen of the memory ranges can be enabled or disabled independently for both read and write cycles.

Table 11. Memory Segments and Their Attributes

Memory Segments	Attributes	Comments
000000h–09FFFFh	Fixed: always mapped to main DRAM	0 to 640 KB – DOS Region
0A0000h–0BFFFFh	Mapped to Hub Interface	Video Buffer (physical DRAM configurable as SMM space)
0C0000h–0C3FFFh	WE RE	Add-on BIOS
0C4000h–0C7FFFh	WE RE	Add-on BIOS
0C8000h–0CBFFFh	WE RE	Add-on BIOS
0CC000h–0CFFFFh	WE RE	Add-on BIOS
0D0000h–0D3FFFh	WE RE	Add-on BIOS
0D4000h–0D7FFFh	WE RE	Add-on BIOS
0D8000h–0DBFFFh	WE RE	Add-on BIOS
0DC000h–0DFFFFh	WE RE	Add-on BIOS
0E0000h–0E3FFFh	WE RE	BIOS Extension
0E4000h–0E7FFFh	WE RE	BIOS Extension
0E8000h–0EBFFFh	WE RE	BIOS Extension
0EC000h–0EFFFFh	WE RE	BIOS Extension
0F0000h–0FFFFFh	WE RE	BIOS Area

MS-DOS Area (00000h–9FFFFh)

The MS-DOS area is 640 KB in size and is always mapped to the main memory controlled by the MCH.

Legacy VGA Ranges (A0000h–BFFFFh)

The legacy 128-KB VGA memory range A0000h–BFFFFh (Frame Buffer) is mapped to the hub interface. This region is also the default for SMM space.

Compatible SMRAM Address Range (A0000h–BFFFFh)

When compatible SMM space is enabled, SMM-mode processor accesses to this range are routed to physical system DRAM at this address. Non-SMM-mode processor accesses to this range are considered to be to the video buffer area as described above. HI originated cycles to enabled SMM space are not allowed and are considered to be to the Video Buffer Area.

Monochrome Adapter (MDA) Range (B0000h–B7FFFh)

Legacy support requires the ability to have a second graphics controller (monochrome) in the system. Accesses in the standard VGA range are forwarded to the hub interface. In addition to the memory range B0000h to B7FFFh, the MCH decodes IO cycles at 3B4h, 3B5h, 3B8h, 3B9h, 3BAh and 3BFh and forwards them to the hub interface.

Expansion Area (C0000h–DFFFFh)

This 128-KB ISA expansion region is divided into eight, 16-KB segments. Each segment can be assigned one of four read/write states: read only, write only, read/write, or disabled. Typically, these blocks are mapped through the MCH and are subtractively decoded to ISA space. Memory that is disabled is not remapped.

Extended System BIOS Area (E0000h–EFFFFh)

This 64-KB area is divided into four, 16-KB segments. Each segment can be assigned independent read and write attributes so it can be mapped either to main system memory or to the hub interface. Typically, this area is used for RAM or ROM. Memory segments that are disabled are not remapped elsewhere.

System BIOS Area (F0000h–FFFFFh)

This area is a single, 64-KB segment. This segment can be assigned read and write attributes. It is by default (after reset) read/write disabled and cycles are forwarded to hub interface. By manipulating the read/write attributes, the MCH can "shadow" BIOS into the main system memory. When disabled, this segment is not remapped.

4.3 Extended Memory Area

This memory area covers 100000h (1 MB) to FFFFFFFFh (4 GB-1) address range and it is divided into the following regions:

- Main System Memory from 1 MB to the Top of Memory; maximum of 4 GB system memory.
- PCI Memory space from the Top of Memory to 4 GB with two specific ranges:
  - APIC Configuration Space from FEC0_0000h (4 GB–20 MB) to FECF_FFFFh and FEE0_0000h to FEEF_FFFFh.
  - High BIOS area from 4 GB to 4 GB–2 MB.

Main System DRAM Address Range (0010_0000h to Top of System Memory)

The address range from 1 MB to the top of system memory is mapped to system memory address range controlled by the MCH. The Top of Main Memory (TOMM) is limited to 4 GB DRAM. All accesses to addresses within this range will be forwarded by the MCH to the system memory unless a hole in this range is created using the fixed hole as controlled by the FDHC register. Accesses within this hole are forwarded to hub interface.

The MCH provides a maximum system memory address decode space of 4 GB. The MCH does not remap APIC memory space. The MCH does not limit system memory address space in hardware.

4.3.1 15 MB–16 MB Window

A hole can be created at 15 MB–16 MB as controlled by the fixed hole enable (FDHC register) in Device 0 space. Accesses within this hole are forwarded to the hub interface. The range of physical system memory disabled by opening the hole is not remapped to the Top of the memory – that physical system memory space is not accessible. This 15 MB–16 MB hole is an optionally enabled ISA hole. Video accelerators originally used this hole. There is no inherent BIOS request for the 15 MB–16 MB hole.

4.3.2 Pre-Allocated Memory

Voids of physical addresses that are not accessible as general system memory and reside within the system memory address range (< TOSM) are created for SMM-mode and legacy VGA graphics compatibility. For VGA graphics compatibility, pre-allocated memory is only required in non-local memory configurations. **It is the responsibility of BIOS to properly initialize these regions**. Table 12 details the location and attributes of the regions. Enabling/Disabling these ranges are described in the MCH Control Register Device 0 (GC).

Table 12. Pre-Allocated Memory

Memory Segments	Attributes	Comments
00000000h–03E7FFFFh	R/W	Available System Memory 62.5 MB
03E80000h–03EFFFFFh	SMM Mode Only - processor Reads	TSEG Address Range
03E80000h–03EFFFFFh	SMM Mode Only - processor Reads	TSEG Pre-allocated Memory

Extended SMRAM Address Range (HSEG and TSEG)

The HSEG and TSEG SMM transaction address spaces reside in this extended memory area.

HSEG

SMM-mode processor accesses to enabled HSEG are remapped to 000A0000h–000BFFFFh. Non-SMM-mode processor accesses to enabled HSEG are considered invalid are terminated immediately on the FSB. The exceptions to this rule are Non-SMM-mode Write Back cycles that are remapped to SMM space to maintain cache coherency. HI originated cycles to enabled SMM space are not allowed. Physical DRAM behind the HSEG transaction address is not remapped and is not accessible.

TSEG

TSEG can be up to 1 MB in size and is the first block after the top of usable physical memory. SMM-mode processor accesses to enabled TSEG access the physical DRAM at the same address. Non-SMM-mode processor accesses to enabled TSEG are considered invalid and are terminated immediately on the FSB. The exceptions to this rule are Non-SMM-mode Write Back cycles that are directed to the physical SMM space to maintain cache coherency. HI originated cycles to enabled SMM space are not allowed.

The size of the SMRAM space is determined by the USMM value in the SMRAM register. When the extended SMRAM space is enabled, non-SMM processor accesses and all other accesses in this range are forwarded to the hub interface. When SMM is enabled, the amount of memory available to the system is equal to the amount of physical DRAM minus the value in the TSEG register.

PCI Memory Address Range (Top of Main Memory to 4 GB)

The address range from the top of main system memory to 4 GB (top of physical memory space supported by the MCH) is normally mapped via the hub interface to PCI.

As an MCH, there is one exception to this rule.

- Addresses decoded to MMIO for DRAM RCOMP configuration registers.

APIC Configuration Space (FEC0_0000h–FECF_FFFFh, FEE0_0000h– FEEF_FFFFh)

This range is reserved for APIC configuration space which includes the default I/O APIC configuration space. The default Local APIC configuration space is FEE0_0000h to FEEF_0FFFh.

Processor accesses to the Local APIC configuration space do not result in external bus activity since the Local APIC configuration space is internal to the processor. However, an MTRR must be programmed to make the Local APIC range uncacheable (UC). The Local APIC base address in each processor should be relocated to the FEC0_0000h (4 GB–20 MB) to FECF_FFFFh range so that one MTRR can be programmed to 64 KB for the Local and I/O APICs. The I/O APIC(s) usually reside in the ICH portion of the chipset or as a stand-alone component(s).

I/O APIC units will be located beginning at the default address FEC0_0000h. The first I/O APIC will be located at FEC0_0000h. Each I/O APIC unit is located at FEC0_x000h where *x* is I/O APIC unit number 0 through F(hex). This address range will be normally mapped to the hub interface.

The address range between the APIC configuration space and the High BIOS (FED0_0000h to FFDF_FFFFh) is always mapped to the Hub Interface.

High BIOS Area (FFE0_0000h -FFFF_FFFFh)

The top 2 MB of the Extended Memory Region is reserved for System BIOS (High BIOS), extended BIOS for PCI devices, and the A20 alias of the system BIOS. The processor begins execution from the High BIOS after reset. This region is mapped to hub interface so that the upper subset of this region aliases to 16 MB–256 KB range. The actual address space required for the BIOS is less than 2 MB but the minimum processor MTRR range for this region is 2 MB so that full 2 MB must be considered.

§

Functional Description 5

This chapter describes the MCH interfaces and functional units including the processor system bus interface, system memory controller, power management, and clocking.

5.1 Processor System Bus

The MCH supports a single Pentium 4 processor with 512-KB L2 cache on 0.13 micron process in a 478-pin package or a processor code named Prescott. The MCH supports FSB frequencies of 400 MHz, 533 MHz, and 800 MHz using a scalable FSB VTT voltage and on-die termination. The MCH supports 32-bit host addressing, decoding up to 4 GB of the processor's memory address space. Host-initiated I/O cycles are decoded to hub interface or MCH configuration space. Host-initiated memory cycles are decoded to hub interface or system memory.

5.1.1 FSB Overview

The MCH supports the Intel® processor subset of the Enhanced Mode Scalable Bus. The cache line size is 64 bytes. Source synchronous transfer is used for the address and data signals. At 100 MHz, 133 MHz, or 200 MHz bus clock, the address signals are double pumped to run at 200 MHz, 266 MHz, or 400 MHz and a new address can be generated every other bus clock. At 100 MHz, 133 MHz, or 200 MHz bus clock, the data signals are quad pumped to run at 400 MHz, 533 MHz, or 800 MHz and an entire 64-B cache line can be transferred in two bus clocks.

The MCH integrates AGTL+ termination resistors on die. The MCH has an IOQ depth of 12. The MCH supports one outstanding deferred transaction on the FSB.

5.1.2 FSB Dynamic Bus Inversion

The MCH supports Dynamic Bus Inversion (DBI) when driving and when receiving data from the processor. DBI limits the number of data signals that are driven to a low voltage on each quad pumped data phase. This decreases the worst-case power consumption of the MCH. DINV[3:0]# indicate if the corresponding 16 bits of data are inverted on the bus for each quad pumped data phase.

DINV[3:0]#	Data Bits
DINV0#	HD[15:0]#
DINV1#	HD[31:16]#
DINV2#	HD[47:32]#
DINV3#	HD[63:48]#

When the processor or the MCH drives data, each 16-bit segment is analyzed. If more than 8 of the 16 signals would normally be driven low on the bus, the corresponding DINV# signal will be asserted and the data will be inverted prior to being driven on the bus. When the processor or the MCH receives data, it monitors DINV[3:0]# to determine if the corresponding data segment should be inverted.

5.1.3 FSB Interrupt Overview

Intel processors support FSB interrupt delivery. They do **not** support the APIC serial bus interrupt delivery mechanism. Interrupt-related messages are encoded on the FSB as “Interrupt Message Transactions.” In the Intel E7210 chipset platform, FSB interrupts may originate from the processor on the system bus, or from a downstream device on the hub interface or AGP. In the later case, the MCH drives the Interrupt Message Transaction onto the system bus.

In the Intel E7210 chipset the ICH contains IOxAPICs, and its interrupts are generated as upstream HI memory writes. Furthermore, PCI 2.3 defines MSI’s (Message Signaled Interrupts) that are also in the form of memory writes. A PCI 2.3 device may generate an interrupt as an MSI cycle on its PCI bus instead of asserting a hardware signal to the IOxAPIC. The MSI may be directed to the IOxAPIC which in turn generates an interrupt as an upstream hub interface memory write. Alternatively, the MSI may be directed directly to the FSB. The target of an MSI is dependent on the address of the interrupt memory write. The MCH forwards inbound HI and AGP/PCI (PCI semantic only) memory writes to address 0FEEx_xxxxh to the FSB as Interrupt Message Transactions.

5.1.3.1 Upstream Interrupt Messages

The MCH accepts message-based interrupts from PCI (**PCI semantics only**) or its hub interface and forwards them to the FSB as Interrupt Message Transactions. The interrupt messages presented to the MCH are in the form of memory writes to address 0FEEx_xxxxh. At the HI or PCI interface, the memory write interrupt message is treated like any other memory write; it is either posted into the inbound data buffer (if space is available) or retried (if data buffer space is not immediately available). Once posted, the memory write from PCI or hub interface to address 0FEEx_xxxxh is decoded as a cycle that needs to be propagated by the MCH to the FSB as an Interrupt Message Transaction.

5.2 System Memory Controller

The MCH can be configured to support DDR266, DDR333, or DDR400 MHz memory in single or dual-channel mode. This includes support for:

- Up to 4 GB of DDR266, DDR333, or DDR400 MHz DDR DRAM.
- DDR266, DDR333, or DDR400 unbuffered 184-pin DDR DRAM DIMMs.
- Up to 2 DIMMs per-channel, single-sided and/or double-sided.
- Byte masking on writes through data masking.

Table 13. System Memory Capacity

DRAM Technology	Smallest Increments	Largest Increments	Maximum Capacity (4 DS DIMMs)
128 Mb	64 MB	256 MB	1024 MB
256 Mb	128 MB	512 MB	2048 MB
512 Mb	256 MB	1024 MB	4096 MB

NOTE: The *Smallest Increments* column also represents the smallest possible single DIMM capacity.

ECC

The MCH supports single-bit Error Correcting Code (or Error Checking and Correcting) on the system memory interface. The MCH generates an 8-bit code word for each 64-bit QWord of memory. Since the code word covers a full QWord, writes of less than a QWord require a read-merge-write operation. Consider a DWord write to memory. In this case, when in ECC mode, the MCH will read the QWord where the addressed DWord will be written, merge in the new DWord, generate a code covering the new QWord and finally write the entire QWord and code back to memory. Any correctable (single-bit) errors detected during the initial QWord read are corrected before merging the new DWord.

DIMM Population Guidelines

DIMM population guidelines are shown in Figure 8 and Figure 9.

Figure 8. Single-Channel Mode Operation

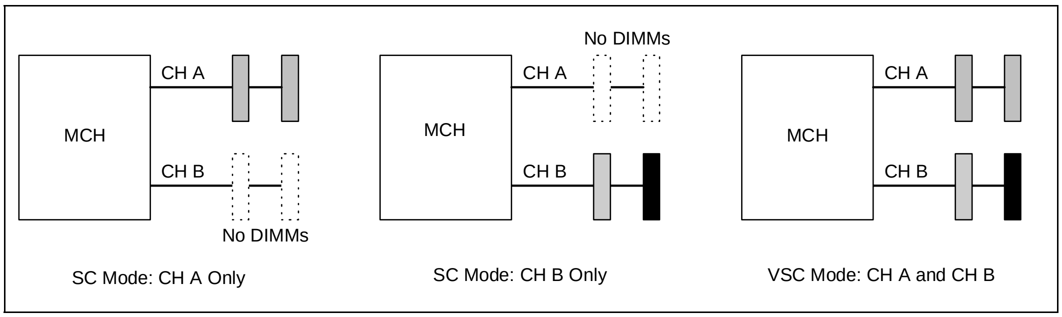
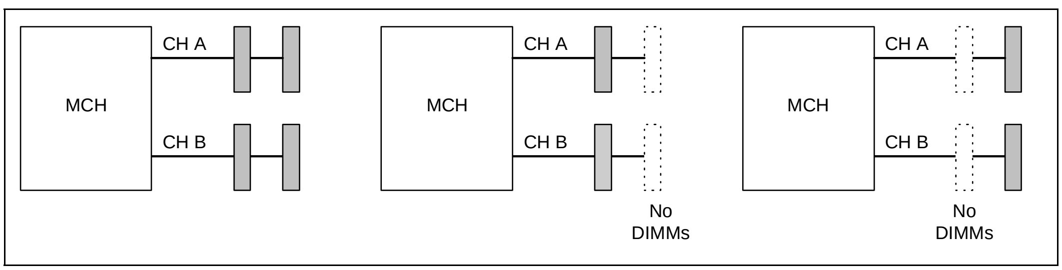


Figure 9. Dual-Channel Mode Operation



5.2.1 DRAM Technologies and Organization

- All standard 128-Mb, 256-Mb and 512-Mb technologies and addressing are supported for x16 and x8 devices.
- All supported devices have four banks.
- The MCH supports page sizes. Page size is individually selected for every row:
  - — 4 KB, 8 KB, and 16 KB for single-channel mode.
  - — 8 KB,16 KB, and 32 KB in dual-channel mode.
- The DRAM sub-system supports a single- or dual-channel, 64 or 72-b (SC) or 128 or 144(DC) wide per-channel.
- There can be a maximum of four rows populated (two double-sided DIMMs) per-channel.
- ECC Support for single-bit error correction and multi-bit error detection.

- Mixed mode DDR DS-DIMMs (x8 and x16 on same DIMM) are not supported.
- By using 512-Mb technology, the largest memory capacity is 2 GB per-channel (64M x 8b x 8 devices x 4 rows = 2 GB).
- By using 128-Mb technology, the smallest memory capacity is 64 MB per-channel (8M x 16b x 4 devices x 1 rows = 64 MB).

Dynamic Addressing Multiplexing Mode

- Baseline addressing is left the same, as a default option.
- Page-coloring addressing is modified, now called “Address-MUXING-dynamic mode,” it is only enabled when the following population rules are met.
- Population rules - Applicable to dynamic mode:
  - Single-/dual-channel mode 1 pair, 2 pairs, or 4 pairs of identical ranks are populated.

5.2.2 Memory Operating Modes

The MCH supports the following modes of operation:

- Single-channel mode (SC):
  - Populate channel A only
  - Populate channel B only
  - Populate both channel A and B
- Dual-channel lock step mode (DS):
  - DS linear mode

The MCH supports a special mode of addressing – dynamic addressing mode. All the above-mentioned modes can be enabled with/without dynamic addressing mode enabled. Table 14 summarizes the different operating modes MCH memory controller can operate.

Table 14. MCH Memory Controller Operating Modes

Mode Type		Dynamic Addressing Mode	Non-Dynamic Addressing Mode
SC Mode	Channel A Only	Yes[1]	Yes
	Channel B Only	Yes[1]	Yes
	Both Channel A & B	Yes[1]	Yes
DS Mode	Linear	Yes	Yes[1]

NOTES:
1. Special cases – need to meet requirements discussed in Section 5.2.2.1.

5.2.2.1 Dynamic Addressing Mode

When the MCH is configured to operate in this mode, FSB-to-memory bus address mapping undergoes a significant change compared to that of a linear operating mode (normal operating mode). In non-dynamic mode, the row selection (row indicates the side of a DIMM) via chip select signals is accomplished based on the size of the row. For example, for a 512 Mb, 16Mx8x4b has a row size of 512 MB selected by CS0# and only four open pages can be maintained for the full

512 MB. This lowers the memory performance (increases read latencies) if most of the memory cycles are targeted to that single row, resulting in opening and closing of accessed pages in that row.

Dynamic addressing mode minimizes the overhead of opening/closing pages in memory banks allowing for row switching to be done less often.

5.2.3 Single-Channel (SC) Mode

If either only channel A or only channel B is populated, then the MCH is set to operate in single-channel mode. Data is accessed in chunks of 64 bits (8B) from the memory channels. If both channels are populated with uneven memory (DIMMs), the MCH defaults to virtual single-channel (VSC) mode. VSC occurs when both channels are populated but the DIMMs are not identical or there is an odd number of identical DIMMs. The MCH behaves identical in both single-channel and virtual single-channel modes (hereafter referred to as single-channel (SC) mode).

In SC mode of operation, the populated DIMMs configuration can be identical or completely different. In addition, for SC mode, not all the slots need to be populated. For example, populating only one DIMM in channel A is a valid configuration for SC mode. Likewise, in VSC mode odd number of slots can be populated. For Dynamic Mode operation, the requirement is to have an even number or rows (side of the DIMM) populated. In SC, dynamic mode operation can be enabled with one single-sided (SS), two SS or two double-sided (DS). For VSC mode, both the channels need to have identical row structures.

5.2.3.1 Linear Mode

This mode is the normal mode of operation for the MCH.

5.2.4 Memory Address Translation and Decoding

The address translation and decoding for the GMCH is provided in Table 15 through Table 18. The supported DIMM configurations are listed in the following bullets. Refer to Section 5.2.5 for details about the configurations being double-sided versus single-sided.

- Technology 128 Mbit – 16M x 8 – page size of 8 KB – row size of 128 MB.
- Technology 128 Mbit – 8M x 16 – page size of 4 KB – row size of 64 MB.
- Technology 256 Mbit – 32M x 8 – page size of 8 KB – row size of 256 MB.
- Technology 256 Mbit – 16M x 16 – page size of 4 KB – row size of 128 MB.
- Technology 512 Mbit – 32M x 16 – page size of 8 KB – row size of 256 MB.
- Technology 512 Mbit – 64M x 8 – page size of 16 KB – row size of 512 MB.

Note: In Table 15 through Table 18 A0, A1, … refers to memory address MA0, MA1, ….
The table cell contents refers to host address signals HAx.

Table 15. DRAM Address Translation (Single-Channel Mode) (Non-Dynamic Mode)

Tech.	Config.	Row size Page size	Row / Column / Bank		Addr	BA1	BA0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
128Mb	8Mx16	64 MB	12x9x2	Row	25	13	12		16	15	14	25	24	23	22	21	20	19	18	17
		4 KB		Col		13	12			AP		11	10	9	8	7	6	5	4	3
128Mb	16Mx8	128 MB	12x10x2	Row	26	14	13		16	15	26	25	24	23	22	21	20	19	18	17
		8 KB		Col		14	13			AP	12	11	10	9	8	7	6	5	4	3
256Mb	16Mx16	128 MB	13x9x2	Row	26	13	12	26	16	15	14	25	24	23	22	21	20	19	18	17
		4 KB		Col		13	12			AP		11	10	9	8	7	6	5	4	3
256Mb	32Mx8	256 MB	13x10x2	Row	27	14	13	27	16	15	26	25	24	23	22	21	20	19	18	17
		8 KB		Col		14	13			AP	12	11	10	9	8	7	6	5	4	3
512Mb	32Mx16	256 MB	13x10x2	Row	27	14	13	27	16	15	26	25	24	23	22	21	20	19	18	17
		8 KB		Col		14	13			AP	12	11	10	9	8	7	6	5	4	3
512Mb	64Mx8	512 MB	13x11x2	Row	28	15	14	28	16	27	26	25	24	23	22	21	20	19	18	17
		16 KB		Col		15	14		13	AP	12	11	10	9	8	7	6	5	4	3

Table 16. DRAM Address Translation (Dual-Channel Mode, Discrete) (Non-Dynamic Mode)

Tech.	Config.	Row size Page size	Row / Column / Bank		Addr	BA1	BA0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
128Mb	8Mx16	64 MB	12x9x2	Row	25	14	13		16	15	26	25	24	23	22	21	20	19	18	17
		4 KB		Col		14	13			AP		12	11	10	9	8	7	6	5	4
128Mb	16Mx8	128 MB	12x10x2	Row	26	14	15		16	27	26	25	24	23	22	21	20	19	18	17
		8 KB		Col		14	15			AP	13	12	11	10	9	8	7	6	5	4
256Mb	16Mx16	128 MB	13x9x2	Row	26	14	13	27	16	15	26	25	24	23	22	21	20	19	18	17
		4 KB		Col		14	13			AP		12	11	10	9	8	7	6	5	4
256Mb	32Mx8	256 MB	13x10x2	Row	27	14	15	28	16	27	26	25	24	23	22	21	20	19	18	17
		8 KB		Col		14	15			AP	13	12	11	10	9	8	7	6	5	4
512Mb	32Mx16	256 MB	13x10x2	Row	27	14	15	28	16	27	26	25	24	23	22	21	20	19	18	17
		8 KB		Col		14	15			AP	13	12	11	10	9	8	7	6	5	4
512Mb	64Mx8	512 MB	13x11x2	Row	28	16	15	28	29	27	26	25	24	23	22	21	20	19	18	17
		16 KB		Col		16	15		14	AP	13	12	11	10	9	8	7	6	5	4

Table 17. DRAM Address Translation (Single-Channel Mode) (Dynamic Mode)

Tech.	Config.	Row size Page size	Row / Column / Bank		Addr	BA1	BA0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
128Mb	8Mx16	64 MB	12x9x2	Row	25	12	18		16	13	14	27	26	23	22	21	25	24	15	17
		4 KB		Col		12	18			AP		11	10	9	8	7	6	5	4	3
128Mb	16Mx8	128 MB	12x10x2	Row	26	18	13		16	14	26	28	27	23	22	21	25	24	15	17
		8 KB		Col		18	13			AP	12	11	10	9	8	7	6	5	4	3
256Mb	16Mx16	128 MB	13x9x2	Row	26	12	18	26	16	13	14	28	27	23	22	21	25	24	15	17
		4 KB		Col		12	18			AP		11	10	9	8	7	6	5	4	3
256Mb	32Mx8	256 MB	13x10x2	Row	27	18	13	27	16	14	26	25	24	23	22	21	29	28	15	17
		8 KB		Col		18	13			AP	12	11	10	9	8	7	6	5	4	3
512Mb	32Mx16	256 MB	13x10x2	Row	27	18	13	27	16	14	26	25	24	23	22	21	29	28	15	17
		8 KB		Col		18	13			AP	12	11	10	9	8	7	6	5	4	3
512Mb	64Mx8	512 MB	13x11x2	Row	28	14	18	28	16	27	26	25	24	23	22	21	30	29	15	17
		16 KB		Col		14	18		13	AP	12	11	10	9	8	7	6	5	4	3

Table 18. DRAM Address Translation (Dual-Channel Mode, Discrete) (Dynamic Mode)

Tech.	Config.	Row size Page size	Row / Column / Bank		Addr	BA1	BA0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
128Mb	8Mx16	64 MB	12x9x2	Row	25	18	13		16	14	26	28	27	23	22	21	25	24	15	17
		4 KB		Col		18	13			AP		12	11	10	9	8	7	6	5	4
128Mb	16Mx8	128 MB	12x10x2	Row	26	14	18		16	27	26	25	24	23	22	21	29	28	15	17
		8 KB		Col		14	18			AP	13	12	11	10	9	8	7	6	5	4
256Mb	16Mx16	128 MB	13x9x2	Row	26	18	13	27	16	14	26	25	24	23	22	21	29	28	15	17
		4 KB		Col		18	13			AP		12	11	10	9	8	7	6	5	4
256Mb	32Mx8	256 MB	13x10x2	Row	27	14	18	28	16	27	26	25	24	23	22	21	30	29	15	17
		8 KB		Col		14	18			AP	13	12	11	10	9	8	7	6	5	4
512Mb	32Mx16	256 MB	13x10x2	Row	27	14	18	28	16	27	26	25	24	23	22	21	30	29	15	17
		8 KB		Col		14	18			AP	13	12	11	10	9	8	7	6	5	4
512Mb	64Mx8	512 MB	13x11x2	Row	28	18	15	28	29	27	26	31	30	23	22	21	25	24	15	17
		16 KB		Col		18	15		14	AP	13	12	11	10	9	8	7	6	5	4

5.2.5 Memory Organization and Configuration

In the following discussion the term “row” refers to a set of memory devices that are simultaneously selected by a chip select signal. The MCH supports a maximum of four rows of memory. For the purposes of this discussion, a “side” of a DIMM is equivalent to a “row” of DRAM devices.

The memory bank address lines and the address lines allow the MCH to support 64-bit wide x8 and x16 DIMMs using 128-Mb, 256-Mb, and 512-Mb DRAM technology.

For the DDR DRAM interface, Table 19 lists the supported configurations. Note that the MCH supports configurations defined in the JEDEC DDR DIMM specification only (A,B,C). Non-JEDEC standard DIMMs (e.g., double-sided x16 DDR DRAM DIMMs) are not supported. More information on DIMM configurations can be found in the *JEDEC DDR DIMM specification*.

Table 19. Supported DDR DIMM Configurations

Density	128 Mbit		256 Mbit		512 Mbit	
Device Width	X8	X16	X8	X16	X8	X16
Single / Double	SS/DS	SS/DS	SS/DS	SS/DS	SS/DS	SS/DS
184 Pin DDR DIMMs	128/256 MB	64 MB/NA	256/512 MB	128 MB/NA	512/1024 MB	256 MB/NA

5.2.6 Configuration Mechanism for DIMMS

Detection of the type of DRAM installed on the DIMM is supported via Serial Presence Detect (SPD) mechanism as defined in the JEDEC DIMM specification. This uses the SCL, SDA, and SA[2:0] pins on the DIMMs to detect the type and size of the installed DIMMs. No special programmable modes are provided on the MCH for detecting the size and type of memory installed. Type and size detection must be done via the serial presence detection pins and is required to configure the MCH.

5.2.6.1 Memory Detection and Initialization

Before any cycles to the memory interface can be supported, the MCH DRAM registers must be initialized. The MCH must be configured for operation with the installed memory types. Detection of memory type and size is accomplished via the System Management Bus (SMBus) interface on the ICH. This two-wire bus is used to extract the DRAM type and size information from the Serial Presence Detect port on the DRAM DIMMs. DRAM DIMMs contain a 5-pin Serial Presence Detect interface, including SCL (serial clock), SDA (serial data), and SA[2:0]. Devices on the SMBus bus have a 7-bit address. For the DRAM DIMMs, the upper four bits are fixed at 1010. The lower three bits are strapped on the SA[2:0] pins. SCL and SDA are connected to the System Management Bus on the ICH. Thus data is read from the Serial Presence Detect port on the DIMMs via a series of I/O cycles to the ICH. BIOS needs to determine the size and type of memory used for each of the rows of memory to properly configure the MCH memory interface.

5.2.6.2 SMBus Configuration and Access of the Serial Presence Detect Ports

For more details, refer to the Intel® *875P/Intel® E7210/Intel® 6300ESB Platform Design Guide*.

5.2.6.3 Memory Register Programming

This section provides an overview of how the required information for programming the DRAM registers is obtained from the Serial Presence Detect ports on the DIMMs. The Serial Presence Detect ports are used to determine Refresh Rate, SMA and SMD Buffer Strength, Row Type (on a row-by-row basis), DRAM Timings, Row sizes, and Row Page sizes. Table 20 lists a subset of the data available through the on board Serial Presence Detect ROM on each DIMM.

Table 20. Data Bytes on DIMM Used for Programming DRAM Registers

Byte	Function
2	Memory type (DDR DRAM)
3	Number of row addresses, not counting bank addresses
4	Number of column addresses
5	Number of banks of DRAM (single- or double-sided DIMM)
11	ECC, non-ECC
12	Refresh rate
17	Number of banks on each device

Table 20 is only a subset of the defined SPD bytes on the DIMMs. These bytes collectively provide enough data for programming the MCH DRAM registers.

5.2.7 Memory Thermal Management

The MCH provides a thermal management method that selectively reduces reads and writes to DRAM when the access rate crosses the allowed thermal threshold.

Read and write thermal management operate independently, and have their own 64-bit register to control operation. Memory reads typically causes power dissipation in the DRAM chips while memory writes typically causes power dissipation in the MCH.

5.2.7.1 Determining When to Thermal Manage

Thermal management may be enabled by one of two mechanisms:

- Software forcing throttling via the SRT (SWT) bit.
- Counter mechanism.

5.3 Power Management

The MCH power management support includes:

- ACPI supported.
- System States: S0, S1 (desktop), S3, S4, S5, C0, C1, C2 (desktop).

5.3.1 Supported ACPI States

The MCH supports the following ACPI States.

- Processor:
  - C0 Full On.
  - C1 Auto Halt.
  - C2-Desktop Stop Grant. Clock to processor still running. Clock stopped to processor core.
- System:
  - G0/S0 Full On.
  - G1/S1 Stop Grant, Desktop S1, same as C2.
  - G1/S2 Not supported.
  - G1/S3 Suspend to RAM (STR). Power and context lost to chipset.
  - G1/S4 Suspend to Disk (STD). All power lost (except wakeup logic on ICH).
  - G2/S5 Soft off. Requires total system reboot.
  - G3 Mechanical Off. All power lost (except real time clock).

5.4 Thermal Management

The MCH implements the following thermal management mechanisms. The mechanisms manage the reads and writes cycles of the system memory interface, thus, ensuring that the temperature can return to the normal operating range.

Hardware-based Thermal Management

The number of hexwords transferred over the DRAM interface are tracked per row. The tracking mechanism takes into account that the DRAM devices consume different levels of power based on cycle type (i.e., page hit/miss/empty). If the programmed threshold is exceeded during a monitoring window, the activity on the DRAM interface is reduced. This helps in lowering the power and temperature.

Software-based Thermal Management

This is used when the external thermal sensor in the system interrupts the processor to engage a software routine for thermal management.

5.4.1 External Thermal Sensor Interface Overview

An external thermal sensor with a serial interface (e.g., the National Semiconductor* LM77, LM87, or other) may be placed next to DDR DIMM (or any other appropriate platform location), or a remote thermal diode may be placed next to the DIMM (or any other appropriate platform location) and connected to the external thermal sensor.

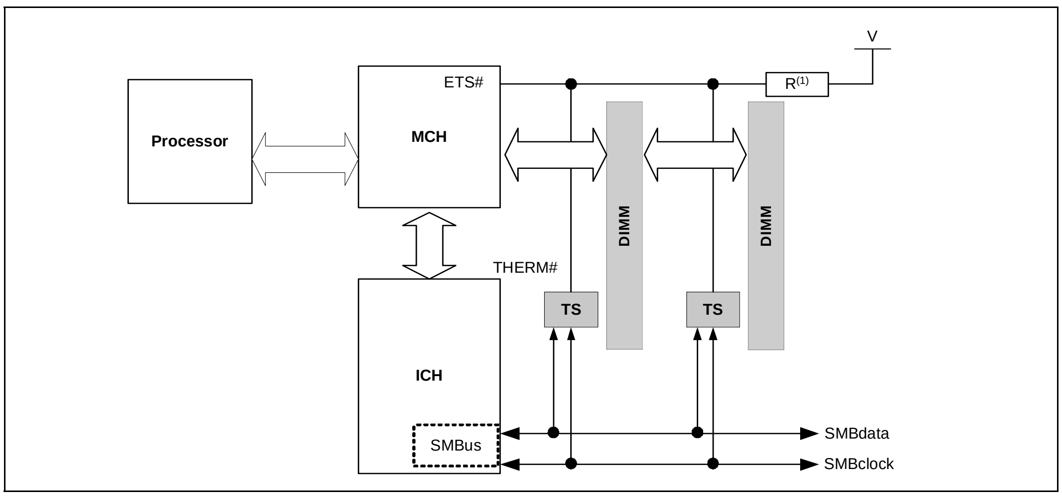
The external sensor can be connected to the ICH via the SMBus interface to allow programming and setup by BIOS software over the serial interface. The external sensor's output should include an active-low open-drain signal indicating an over-temp condition (e.g., LM77 T_CRIT# or INT#

in comparator mode). The sensor's output remains asserted for as long as the over-temp condition exists and deasserts when the temperature has returned to within normal operating range. This external sensor output will be connected to the MCH input (EXTTS#) and will trigger a preset interrupt and/or read-throttle on a level-sensitive basis.

Additional external thermal sensor's outputs, for multiple sensors, can be wire-OR'd together allow signaling from multiple sensors located physically separately. Software can, if necessary, distinguish which DIMM(s) is the source of the over-temp through the serial interface. However, since the DIMMs will be located on the same memory bus data lines, any MCH-base read throttle will apply equally.

Note: The use of external sensors that include an internal pull-up resistor on the open-drain thermal trip output is discouraged; however, it may be possible depending on the size of the pull-up and the voltage of the sensor.

Figure 10. Platform External Sensor



NOTE: External pull-up R is associated with the voltage rail of the MCH input.

5.4.1.1 External Thermal Sensor Usage Model

There are several possible usage models for an external thermal sensor:

- External sensor(s) used for characterization only, not for normal production.
- Sensor on the DIMMs for temperature in OEM platform and use the results to permanently set read throttle values in the BIOS.
- Sensor on the MCH for temperature in OEM platform and use the results to permanently set write throttle values in the BIOS.
- External sensor(s) used for dynamic temperature feedback Control in production releases.
- Sensor on DIMMs, which can be used to dynamically control read throttling.
- Sensor on MCH, which can be used to dynamically control write throttling.

The advantage of the characterization model is the Bill-of-Material (BOM) cost; whereas, the potential advantage of the dynamic model is that retail customers may be able to experience higher peak performance since the throttle values are not forced to encompass worse case environmental conditions.

Characterization tools (e.g., CTMI and Maxband) can be made to work either with external or internal sensors.

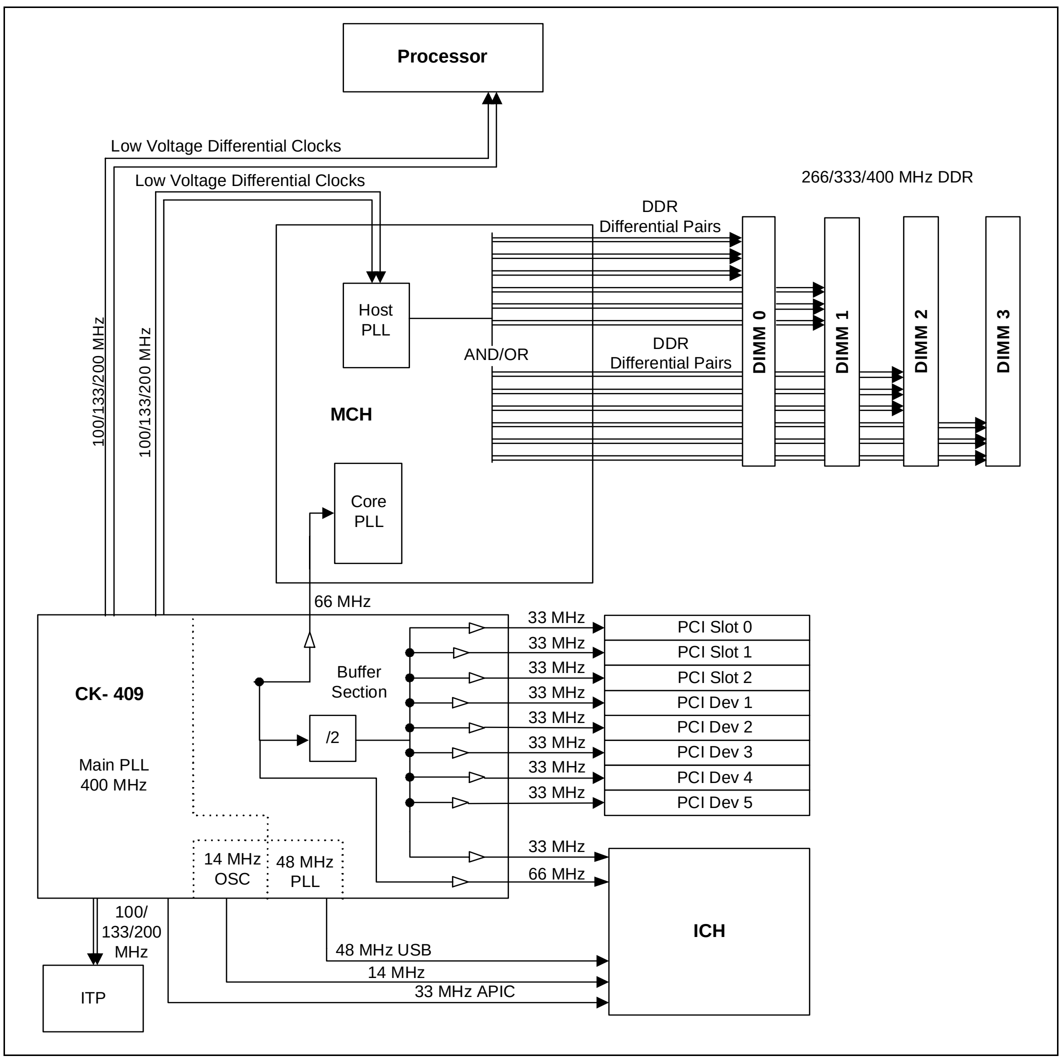
5.5 Clocking

The MCH has the following clocks:

- 100/133/200 MHz spread spectrum, low voltage (0.7 V) differential HCLKP/HCLKN for FSB.
- 66.667 MHz, spread spectrum, 3.3 V GCLKIN for hub interface.
- 48 MHz, non-spread spectrum, USB clock.
- 12 pairs DRAM output clocks (SCMCLK_x[5:0] and SCMDCLK_x[5:0]# for both channels A and B).

The MCH has inputs for a low voltage, differential pair of clocks called HCLKP and HCLKN. These pins receive a host clock from the external clock synthesizer. This clock is used by the host interface and system memory logic (Host Clock Domain). Hub interface is driven off of the 66-MHz clock.

Figure 11. Intel® E7210 Chipset System Clock Block Diagram



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Electrical Characteristics 6

This chapter contains the maximum ratings, thermal characteristics, power characteristics, and DC characteristics for the MCH.

6.1 Absolute Maximum Ratings

Table 21 lists the MCH's maximum environmental stress ratings. Functional operation at the absolute maximum and minimum is neither implied nor guaranteed. Functional operating parameters are listed in the DC Characteristics tables.

Warning: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operating beyond the "operating conditions" is not recommended and extended exposure beyond "operating conditions" may affect reliability.

Table 21. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
VCC	1.5 V Core Supply	-0.3	1.75	V
VCC_HI	1.5 V HI/CSA Supply	-0.3	1.75	V
VTT	VTT Supply	-0.3	1.75	V
VCC_DDR	2.6 V DDR System Memory Interface Supply	-0.5	3	V
VCCA_DDR	1.5 V Analog Supply for System Memory PLLs	-0.3	1.75	V
VCC_33	3.3 V Supply	-0.3	3.6	V
VCCA_FSB	1.5 V Host PLL Analog Supply	-0.3	1.75	V

6.2 Thermal Characteristics

Refer to the *Intel® E7210 Chipset Thermal Design Guide* for all thermal characteristics.

6.3 Power Characteristics

Table 22. Power Characteristics

Symbol	Parameter	Max	Unit	Notes
I_{VCC}	1.5 V Core Supply Current	2.7	A	1
I_{VCC_HI}	1.5 V HI/CSA Supply Current	0.18	A	1
I_{VTT}	VTT Supply Current	1.6	A	
I_{VCC_DDR}	2.6 V DDR System Memory Interface Supply Current	6.27	A	
I_{VCCA_DDR}	1.5 V Analog Supply Current for System Memory DLLs	1.2	A	

Table 22. Power Characteristics (Continued)

Symbol	Parameter	Max	Unit	Notes
I_{VCC_33}	3.3 V Supply Current	0.2	A	
I_{VCCA_FSB}	1.5 V Host PLL Analog Supply Current	0.05	A	
$I_{VCC\_SUS\_2.6}$	2.6 V Standby Supply Current	0.250	A	

NOTE: VCC and VCC_HI current levels may happen simultaneously and can be summed into one 1.5 V supply.

6.4 Signal Groups

The signal description includes the type of buffer used for the particular signal:

AGTL+ Open Drain AGTL+ interface signal. Refer to the AGTL+ I/O Specification for complete details. The MCH integrates most AGTL+ termination resistors.

HI15 Hub Interface and CSA 1.5 V CMOS buffers.

SSTL_2 Stub Series Terminated Logic 2.6 V compatible signals. DDR system memory 2.6 V CMOS buffers.

Miscellaneous 2.6 V and 3.3 V miscellaneous buffers.

Table 23. Signal Groups

Signal Group	Signal Type	Signals	Notes[1]
Hub Interface Signal Groups			
(e)	Hub Interface CMOS I/O	HI[10:0], HISTRS, HISTRF	
(f)	Hub Interface Miscellaneous	HI_SWING, HI_VREF, HI_RCOMP	
CSA Interface Signal Groups			
(e)	CSA Interface CMOS I/O	CI[10:0], CISTRS, CISTRF	
(f)	CSA Interface Miscellaneous	CI_SWING, CI_VREF, CI_RCOMP	
Host Interface Signal Groups			
(g)	AGTL+ I/O	ADS#, BNR#, DBSY#, DINV[3:0]#, DRDY#, HA[31:3]#, HADSTB[1:0] #, HD[63:0]#,HDSTBP[3:0]#, HDSTBN[3:0]#, HIT#, HITM#, HREQ[4:0]#, PROCHOT#	
(h)	AGTL+ Input	HLOCK#	
(i)	AGTL+ Output	BPRI#, BREQ0#, CPURST#, DEFER#, HTRDY#, RS[2:0]#	
(j)	Host Clock Input	HCLKP, HCLKN	
(k)	Host Miscellaneous	HDVREF[1:0], HDRCOMP, HDSWING	
DDR Interface Signal Groups			
(l)	DDR SSTL_2 I/O	SDQ_A[63:0], SDQ_B[63:0], SDQS_A[8:0], SDQS_B[8:0], SECC_A[7:0], SECC_B[7:0]	
(m)	DDR SSTL_2 Output	SCMDCLK_A[5:0], SCMDCLK_B[5:0], SCMDCLK_A[5:0]#, SCMDCLK_B[5:0]#, SMAA_A[12:0], SMAA_B[12:0], SBA_A[1:0], SBA_B[1:0], SRAS_A#, SRAS_B#, SCAS_A#, SCAS_B#, SWE_A#, SWE_B#, SCS_A[3:0]#, SCS_B[3:0]#, SCKE_A[3:0], SCKE_B[3:0]	

Table 23. Signal Groups (Continued)

Signal Group	Signal Type	Signals	Notes[1]
(v)	DDR RCOMP	SMXRCOMP, SMYRCOMP	
(n)	DDR Miscellaneous[2]	SMXRCOMPVOL, SMXRCOMPVOH, SMYRCOMPVOL, SMYRCOMPVOH, SMVREF_A, SMVREF_B	
Reset and Miscellaneous Signal Groups			
(t)	2.6 V Miscellaneous Input (3.3V tolerant)	RSTIN#, PWROK, EXTTS#	
(w)	XOR Test pins	TESTP[29:0]	
(x)	Bus Select Inputs	BSEL[1:0]	
(y)	Clock pin	GCLKIN	

NOTES:
1. For details on BSEL[1:0] pin electrical requirements, see the *Intel® E7210 Chipset Platform Design Guide.*
2. For additional details on SMXRCOMP, SMYRCOMP, SMXRCOMPVOL, SMXRCOMPVOH, SMYRCOMPVOL, SMYRCOMPVOH pin electrical requirements see the *Intel® E7210 Chipset Platform Design Guide*.

6.5 DC Parameters

Unless otherwise specified, all DC operating conditions are specified at the pin.

Table 24. DC Operating Characteristics

Signal Name	Parameter	Min	Nom	Max	Unit
I/O Buffer Supply Voltage					
VCC	Core Voltage	1.425	1.5	1.575	V
VCC_HI	HI/CSA I/O Voltage	1.425	1.5	1.575	V
VTT (Pentium 4 processor only)	Host AGTL+ Termination Voltage	1.35	1.45	1.55	V
VTT (processor code named Prescott only)	Host AGTL+ Termination Voltage	1.14	1.225	1.31	V
VCC_DDR	DDR I/O Supply Voltage	2.5	2.6	2.7	V
VCCA_DDR	Analog DDR Supply Voltage	1.425	1.5	1.575	V
VCC_3_3	3.3V Supply Voltage	3.135	3.3	3.465	V
VCCA_FSB	Host PLL Analog Voltage	1.425	1.5	1.575	V
Reference Voltages					
HI_VREF[6, 7]	Hub Interface Reference Voltage	0.343	0.35	0.357	V
HI_SWING[6, 8]	Hub Interface Compensation Reference Voltage	0.784	0.8	0.816	V

Table 24. DC Operating Characteristics (Continued)

Signal Name	Parameter	Min	Nom	Max	Unit
CI_VREF[9, 10]	CSA Interface Reference Voltage	0.343	0.35	0.357	V
CI_SWING[9, 11]	CSA Interface Compensation Reference Voltage	0.784	0.8	0.816	V
Vsh[1]	MCH Vtt/CPU Shared Voltage	(Vtt_min + VccCPU_min)/2	(Vtt + VccCPU)/2	(Vtt_max + VccCPU_max)/2	V
HDVREF[2]	Vtt Plane Host Reference Voltage	0.63 x Vsh_min – 2%	0.63 x Vsh	0.63 x Vsh_max + 2%	V
HDSWING/ HASWING	Host Compensation Reference Voltage	1/4 x Vtt_min – 2%	1/4 x Vtt	1/4 x Vtt_max + 2%	V
SMXRCOMPVOL[3]/ SMYRCOMPVOL	DDR RCOMP VOL	VCC_DDR_min * (1/4.112) – 2%	VCC_DDR * (1/4.112)	VCC_DDR_max * (1/4.112) + 2%	V
SMXRCOMPVOH[3]/ SMYRCOMPVOH	DDR RCOMP VOH	VCC_DDR_min * (3.112/4.112) – 2%	VCC_DDR * (3.112/4.112)	VCC_DDR_max * (3.112/4.112) + 2%	V
SMVREF	DDR Reference Voltage	0.49 x VCC_DDR_min	0.5 x VCC_DDR	0.51 x VCC_DDR_max	V

NOTES:
1. Refer to the appropriate processor datasheet for processor VCC values used to calculate Vsh.
2. HDVREF is generically referred to as GTLREF throughout the rest of this document.
3. SMXRCOMPVOL/SMYRCOMPVOL and SMXRCOMPVOH/SMYRCOMPVOH have maximum input leakage current of 1 mA.
4. Measured at receiver pad.
5. Standard 50 Ω load to ground.
6. HI_REF and HI_SWING are derived from VCC (nominal VCC = 1.5 V) which is the nominal core voltage for the MCH. Voltage supply tolerance for a particular interface driver voltage must be within a 5% range of nominal.
7. Nominal value of HI_REF is 0.350 V. The specification is at nominal VCC. Note that HI_REF will vary linearly with VCC; thus, VCC variation (± 5%) must be accounted for in the HI_REF specification in addition to the 2% variation of HI_REF in the table.
8. Nominal value of HI_SWING is 0.800 V. The specification is at nominal VCC. Note that HI_SWING will vary linearly with VCC; thus, VCC variation (± 5%) must be accounted for in the HI_SWING specification in addition to the 2% variation of HI_SWING in the table.
9. CI_REF and CI_SWING are derived from VCC (nominal VCC = 1.5 V) which is the nominal core voltage for the MCH. Voltage supply tolerance for a particular interface driver voltage must be within a 5% range of nominal.
10. Nominal value of CI_VREF is 0.350 V. The specification is at nominal VCC. Note that CI_VREF will vary linearly with VCC; thus, VCC variation (± 5%) must be accounted for in the CI_VREF specification in addition to the 2% variation of CI_REF in the table.
11. Nominal value of CI_SWING is 0.800 V. The specification is at nominal VCC. Note that CI_SWING will vary linearly with VCC; thus, VCC variation (± 5%) must be accounted for in the CI_SWING specification in addition to the 2% variation of CI_SWING in the table.

Table 25. DC Characteristics

Symbol	Signal Group	Parameter	Min	Nom	Max	Unit	Notes
1.5 V Hub Interface							
V_{IL_HI}	(e)	Hub Interface Input Low Voltage	-0.3		HI_VREF – 0.1	V	
V_{IH_HI}	(e)	Hub Interface Input High Voltage	HI_VREF + 0.1		1.2	V	
V_{OL_HI}	(e)	Hub Interface Output Low Voltage			0.05	V	I_{OL} = 1 mA
V_{OH_HI}	(e)	Hub Interface Output High Voltage	0.6		1.2	V	$I_{OUT} = 0.8/R_{TT}$, R_{TT} = 60 Ω
I_{LEAK_HI}[7]	(e)	Hub Interface Input Leakage Current			± 50	µA	

Table 25. DC Characteristics (Continued)

Symbol	Signal Group	Parameter	Min	Nom	Max	Unit	Notes
C_{IN_HI}	(e)	Hub Interface Input Capacitance			5	pF	F_C = 1 MHz
1.5 V CSA Interface							
V_{IL_CI}	(e)	CSA Interface Input Low Voltage	–0.3		CI_VREF – 0.1	V	
V_{IH_CI}	(e)	CSA Interface Input High Voltage	CI_VREF + 0.1		1.2	V	
V_{OL_CI}	(e)	CSA Interface Output Low Voltage			0.05	V	I_{OL} = 1 mA
V_{OH_CI}	(e)	CSA Interface Output High Voltage	0.6		1.2	V	$I_{OUT} = 0.8/R_{TT}$, R_{TT} = 60 Ω
I_{LEAK_CI}[8]	(e)	CSA Interface Input Leakage Current			± 50	µA	
C_{IN_CI}	(e)	CSA Interface Input Capacitance			5	pF	F_C = 1 MHz
VTT DC Characteristics							
V_{IL_AGTL+}	(g,h)	Host AGTL+ Input Low Voltage			HDVREF – (0.04*Vsh)	V	
V_{IH_AGTL+}	(g,h)	Host AGTL+ Input High Voltage	HDVREF + (0.04*Vsh)			V	
V_{OL_AGTL+}	(g,i)	Host AGTL+ Output Low Voltage		1/4* Vsh		V	
V_{OH_AGTL+}	(g,i)	Host AGTL+ Output High Voltage	(Vsh–0.1) * 0.95		Vsh	V	
I_{OL_AGTL+}	(g,i)	Host AGTL+ Output Low Current			0.75 * Vshmax / Rttmin	mA	Rtt_{min} = 57 Ω
I_{LEAK_AGTL+}	(g,h)	Host AGTL+ Input Leakage Current			± 25	µA	V_{OL}<Vpad<Vtt
C_{PAD_AGTL+}	(g,h)	Host AGTL+ Input Capacitance	1		3.3	pF	F_C = 1 MHz
2.6 V DDR System Memory							
$V_{IL\_DDR(DC)}$	(l)	DDR Input Low Voltage	–0.1 * VCC_DDR		SMVREF – 0.15	V	
$V_{IH\_DDR(DC)}$	(l)	DDR Input High Voltage	SMVREF + 0.15		VCC_DDR	V	
$V_{IL\_DDR(AC)}$	(l)	DDR Input Low Voltage	–0.1 * VCC_DDR		SMVREF – 0.31	V	
$V_{IH\_DDR(AC)}$	(l)	DDR Input High Voltage	SMVREF + 0.31		VCC_DDR	V	
V_{OL_DDR}	(l,m,v)	DDR Output Low Voltage			0.600	V	With 50 Ω load to DDR Vtt
V_{OH_DDR}	(l,m,v)	DDR Output High Voltage	VCC_DDR – 0.600			V	With 50 Ω load to DDR Vtt
I_{OL_DDR}	(l,m)	DDR Output Low Current			25	mA	With 50 Ω load to DDR Vtt
I_{OH_DDR}	(l,m)	DDR Output High Current	–25			mA	With 50 Ω load to DDR Vtt

Table 25. DC Characteristics (Continued)

Symbol	Signal Group	Parameter	Min	Nom	Max	Unit	Notes
$I_{OL\_DDR RCOMP}$	(v)	DDR RCOMP Output Low Current			50	mA	
$I_{OH\_DDR RCOMP}$	(v)	DDR RCOMP Output High Current	–50			mA	
I_{Leak_DDR}	(l)	Input Leakage Current			±15	µA	
C_{IN_DDR}	(l)	DDR Input /Output Pin Capacitance			5.5	pF	F_C = 1 MHz
2.6 V Miscellaneous Signals (3.3 V tolerant)							
V_{IL}	(t)	2.6 V Input Low Voltage			0.4	V	
V_{IH}	(t)	2.6 V Input High Voltage	VCC_DDR – 0.4		VCC_33	V	
I_{LEAK}	(t)	2.6 V Input Leakage Current			±50	µA	
C_{IN}	(t)	2.6 V Input Capacitance			5.5	pF	
Bus Select Signals							
V_{IL}	(x)	Input Low Voltage			0.4	V	
V_{IH}	(x)	Input High Voltage	0.8			V	
Clock Signals							
V_{IL}	(y)	Input Low Voltage			0.4	V	
V_{IH}	(y)	Input High Voltage	VCC_DDR – 0.4		VCC_33	V	1
I_{LEAK}	(y)	Input Leakage Current			100	µA	
C_{IN}	(y)	Input Capacitance			5.5	pF	
$V_{CROSS(abs)}$	(j)	Absolute Crossing Voltage	0.250	NA	0.550	V	2, 3
$V_{CROSS(rel)}$	(j)	Relative Crossing Voltage	0.250 + 0.5(V_{Havg} – 0.700)	NA	0.550 + 0.5(V_{Havg} – 0.700)	V	3, 4, 5

NOTES:
1. Absolute max overshoot = 4.5 V.
2. Crossing voltage is defined as the instantaneous voltage value when the rising edge of HCLKP equals the falling edge of HCLKN.
3. The crossing point must meet the absolute and relative crossing point specifications simultaneously.
4. V_{Havg} is the statistical average of the V_H measured by the oscilloscope.
5. V_{Havg} can be measured directly using “Vtop” on Agilent* oscilloscopes and “High” on Tektronix* oscilloscopes.
6. Maximum leakage current specification for HI_VREF and HI_SWING pins is 50 µA. Refer to the *Intel® E7210 Chipset Platform Design Guide* for the resistor divider circuit details that take this specification into account.
7. Maximum leakage current specification for CI_VREF and CI_SWING pins is 50 µA. Refer to the *Intel® E7210 Chipset Platform Design Guide* for the resistor divider circuit details that takes this specification into account.

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Ballout and Package Information 7

This chapter provides the MCH ballout and package information.

7.1 MCH Ballout

The ballout footprint is shown in Figure 12 and Figure 13. These figures represent the ballout arranged by ball number. Table 26 provides the ballout arranged alphabetically by signal name.

Note: The following notes apply to the ballout:

1. NC = No Connect.
2. RSVD = These reserved balls should not be connected and should be allowed to float.
3. Shaded cells in Figure 12 and Figure 13 do not have a ball.

Figure 12. MCH Ballout Diagram (Top View—Left Side)

	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17
AN			NC	VCC_DDR	SDQ_A24	SMAA_A5	SDQ_A22	SMAA_A11	SDQ_A17	SDQ_A20	SCKE_A3	VCC_DDR	SDQ_A15	SCMDCLK _A1	SDQ_A13	VCC_DDR	SDQ_A9
AM		NC	RSVD	TESTP14	VSS	SDQ_A19	SMAA_A7	VSS	SDQ_A21	SCKE_A0	VSS	SDQ_A11	SCMD CLK_A1#	VSS	SCMD CLK_A4	TESTP18	VSS
AL	NC	RSVD	VSS	SDQS_A3	SDQ_A25	SDQ_A23	SMAA_A8	SMAA_A9	SDQS_A2	SMAA_ A12	SCKE_A2	SCKE_A1	SDQ_A10	SMAA_ B12	SCMD CLK_A4#	SDQ_A12	SDQ_A8
AK	VCCA_ DDR	TESTP26	SDQ_A30	SMAA_A4	TESTP13	SMAA_A6	VSS	SDQ_A18	VSS	SDQ_A16	TESTP28	TESTP15	TESTP29	SDQ_A14	VSS	SDQ_B10	VSS
AJ	SECC_A4	VSS	SDQ_A26	VSS	SMAA_A3	SDQ_A29	SDQ_A28	SDQ_B25	SDQ_B24	SDQ_B23	SDQ_B22	SMAA_B9	SDQS_B2	SDQ_B20	SDQS_A1	SDQ_B15	SDQ_A2
AH	SECC_A5	SMAA_A1	SDQ_A31	SDQ_A27	SMAA_B1	VSS	SMAA_B3	TESTP6	TESTP27	TESTP20	SDQ_B18	VSS	SDQ_B17	TESTP19	SCKE_B3	VSS	SCMD CLK_B4#
AG	SCMD CLK_A3#	SCMDCLK _A3	SMAA_A2	SECC_A0	SMAA_B2	SDQ_B31	SDQ_B26	SDQS_B3	SMAA_B6	SDQ_B19	SMAA_B7	SMAA_B11	SDQ_B16	SCKE_B2	SDQ_B14	SCMD CLK_B1	SCMD CLK_B4
AF	SDQS_A8	VSS	SECC_A1	VSS	SECC_B1	TESTP7	SMAA_B4	VSS	SDQ_B28	SMAA_B5	VSS	SDQ_B21	SCKE_B1	VSS	TESTP16	SCMD CLK_B1#	VSS
AE	SECC_A2	SCMD CLK_A0#	SCMD CLK_A0	TESTP12	SCMDCLK _B0	SECC_B0	SECC_B4	SDQ_B30	SDQ_B29	VSS	SMAA_B8	VSS	SCKE_B0	VSS	SDQ_B11	VSS	SDQ_B13
AD	VCC_DDR	SECC_B6	SMY RCOMP	SMAA_ A10	SCMD CLK_B0#	VSS	SCMD CLK_B3	SDQ_B27	VSS	VCC_DDR	VSS	VCC_DDR	VSS	VCC_DDR	VSS	VCC_DDR	VSS
AC	SECC_A3	VSS	SECC_A6	VSS	SMAA_A0	SDQS_B8	SCMD CLK_B3#	TESTP25	SECC_B5	VSS	VCCA_ DDR	VCCA_ DDR	VCC_DDR	VSS	VCC_DDR	VSS	VCC_DDR
AB	SECC_A7	TESTP21	SBA_B1	SBA_A1	SECC_B7	VSS	SECC_B2	SMAA_B0	VSS	VCC_DDR	VCCA_ DDR						
AA	SDQ_A33	SDQ_A37	SDQ_A36	SDQS_A4	SDQ_B33	SDQ_A32	SECC_B3	VSS	SMAA_ B10	VSS	VCC_DDR						
Y	SDQ_A34	VSS	SDQ_A38	VSS	SDQ_B37	VSS	SDQ_B36	SDQ_B32	VSS	VCC_DDR	VSS			VCC	VSS	VCC	VSS
W	SDQ_A39	SDQ_A35	SBA_A0	TESTP8	SDQ_B39	SDQ_B38	SDQ_B34	VSS	SDQS_B4	VSS	VCC_DDR			VSS	VCC	VSS	VCC
V	SDQ_A40	VSS	SRAS_A#	SDQ_A44	SDQ_B44	VSS	SDQ_B35	SBA_B0	VSS	VCC_DDR	VSS			VCC	VSS	VCC	VSS
U	SDQ_A45	SDQ_A41	SWE_A#	TESTP9	SWE_B#	SRAS_B#	SDQ_B40	VSS	SDQ_B45	VSS	VCC_DDR			VSS	VCC	VSS	VCC
T	SCAS_A#	TESTP22	SCS_A0#	SCS_A2#	SCS_B1#	VSS	SCS_B2#	SDQ_B41	VSS	VCC_DDR	VSS			VCC	VSS	VCC	VSS
R	SCS_A3#	VSS	SDQS_A5	VSS	SDQ_B46	SDQS_B5	SCS_B3#	TESTP10	SCAS_B#	VSS	VCC_DDR			VSS	VCC	VSS	VCC
P	VCC_DDR	SCS_A1#	SDQ_A42	SDQ_B47	SDQ_B52	VSS	SDQ_B42	SCS_B0#	VSS	VCC_DDR	VSS			VCC	VSS	VCC	VSS
N	SMYRCO MPVOL	SMYRCO MPVOH	SDQ_A43	VSS	SDQ_B48	SDQ_B53	SDQ_B49	TESTP11	SDQ_B43	VSS	VCC_DDR						
M	SDQ_A47	VSS	SDQ_A46	SCMD CLK_B2	SCMD CLK_B2#	VSS	SCMD CLK_B5#	SCMD CLK_B5	VSS	VSS	VSS						
L	SDQ_A52	SDQ_A49	SDQ_A48	TESTP23	SDQS_B6	SDQ_B54	SDQ_B55	VSS	SDQ_B51	VSS	VSS	VTT	VTT	VTT	VTT	VTT	VTT
K	SDQ_A53	VSS	SCMD CLK_A5#	SCMD CLK_A5	SDQ_B50	VSS	SDQ_B56	SDQS_B7	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
J	SCMD CLK_A2#	SCMD CLK_A2	SDQS_A6	VSS	SDQ_B60	SDQ_B61	SDQ_B62	VSS	VSS	VSS	VSS	VSS	HD16#	VSS	HD48#	VSS	DINV3#
H	SDQ_A54	VSS	SDQ_A55	SDQ_A50	SDQ_B57	VSS	SDQ_B59	VSS	VSS	HD19#	HD17#	HD21#	VSS	HD18#	VSS	CPURST#	VSS
G	SDQ_A51	SDQ_A60	SDQ_A61	VSS	SDQ_B58	SDQ_B63	VSS	HD20#	HD23#	HD27#	HD22#	HD29#	HD24#	HD49#	HDSTB P3#	HD53#	HD62#
F	SDQ_A56	VSS	SDQ_A57	SDQS_A7	VSS	VSS	VSS	VSS	DINV1#	VSS	HD28#	VSS	HDSTB P1#	VSS	HDSTB N3#	VSS	HD55#
E	SDQ_A62	SDQ_A63	SDQ_A59	VSS	TESTP24	HD4#	HD3#	HDSTB P0#	HD26#	HD25#	HD30#	HDSTB N1#	HD31#	HD50#	HD52#	HD51#	HD54#
D	VCC_DDR	VSS	SDQ_A58	VSS	VSS	HD1#	VSS	HD10#	VSS	HD36#	VSS	HDSTB P2#	VSS	HD40#	VSS	HD46#	VSS
C	NC	SMVREF_ A	VSS	VSS	HD0#	HD6#	HD5#	HD11#	HD15#	HD34#	HD33#	HD37#	HD38#	DINV2#	HD45#	HD44#	HA18#
B		NC	DINV0#	VSS	HD7#	VSS	HD9#	VSS	HD12#	VSS	HDSTB N2#	VSS	HD41#	VSS	HD43#	VSS	HA19#
A			NC	VCCA_ FSB	HD8#	HD2#	HD13#	HDSTB N0#	HD14#	VTT	HD32#	HD39#	HD35#	VTT	HD42#	HD47#	HA17#
	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17

Figure 13. MCH Ballout Diagram (Top View—Right Side)

16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
SDQ_A7	SDQS_A0	SDQ_A4	SMXRCOMPVOH	SMVREF_B	VCC_DDR	VCC_DDR	RSVD	VCC_HI	HI7	HI4	VCC_HI	HI9	NC			AN
SDQ_A3	SDQ_A1	VSS	SDQ_B5	VCC_DDR	VCC_DDR	VCC_DDR	VSS	HI6	VSS	HI10	VSS	HI2	VSS	NC		AM
SDQ_A6	SDQ_A0	SDQS_B0	SDQ_B1	VCC_DDR	VCC_DDR	VCC_DDR	CI2	HI5	HI8	VSS	HISTRS	HI0	VSS	VSS	NC	AL
SDQ_A5	VSS	SDQ_B2	TESTP4	VCC_DDR	VCC_DDR	VCC_DDR	CI1	VSS	CISTRF	HISTRF	HI1	VSS	TESTP35	TESTP33	TESTP32	AK
SDQ_B12	SDQ_B3	SDQ_B6	SDQ_B4	VCC_DDR	VCC_DDR	VCC_DDR	VSS	CISTRS	VSS	HI3	VSS	TESTP37	TESTP36	VSS	TESTP34	AJ
TESTP5	SDQ_B7	VSS	SMXRCOMPVOL	VCC_DDR	VCC_DDR	VCC_DDR	CI3	CI10	CI8	VSS	CI7	VSS	VSS	TESTP38	TESTP39	AH
SDQ_B9	SDQ_B8	SDQ_B0	SMXRCOMP	VCC_DDR	VCC_DDR	VCC_DDR	CI0	RSVD	VSS	CI6	VSS	TESTP68	TESTP66	VSS	CI_VREF	AG
SDQS_B1	VSS	EXTTS#	VSS	VCC_DDR	VCC_DDR	VCC_DDR	VSS	VSS	CI4	CI5	TESTP40	VSS	TESTP64	CI_RCOMP	HI_VREF	AF
VSS	VCC_DDR	VSS	TESTP17	VCC_DDR	VCC_DDR	VCC_DDR	PWROK	RSTIN#	CI9	VSS	TESTP42	TESTP41	CI_SWING	VSS	VCC	AE
VCC_DDR	VSS	VCC_DDR	VSS	VCC_DDR	VCC_DDR	VCC_DDR	VSS	TESTP45	VSS	TESTP44	TESTP43	VSS	HI_SWING	GVREF	HI_RCOMP	AD
VSS	VCC_DDR	VSS	VCC_DDR	VCC_DDR	VCC_DDR	VCC_DDR	RSVD	TESTP47	RSVD	VSS	TESTP69	TESTP46	TESTP78	VSS	TESTP95	AC
					VSS	VSS	VSS	VSS	TESTP73	TESTP75	TESTP93	VSS	TESTP76	TESTP72	TESTP94	AB
					VSS	VCC_HI	VSS	TESTP84	TESTP87	VSS	TESTP86	TESTP48	TESTP70	VSS	VCC	AA
VCC	VSS	VCC			VCC_HI	VCC_HI	VCC_HI	VSS	TESTP82	TESTP88	TESTP85	VSS	TESTP52	TESTP49	TESTP50	Y
VSS	VCC	VSS			VCC_HI	VCC_HI	VCC_HI	TESTP92	TESTP83	VSS	TESTP89	TESTP53	TESTP54	VSS	TESTP51	W
VCC	VSS	VCC			VCC	VCC_HI	VCC_HI	VSS	TESTP77	TESTP81	TESTP80	VSS	TESTP71	TESTP67	TESTP65	V
VSS	VCC	VSS			VCC	VCC_HI	VCC_HI	TESTP91	TESTP90	VSS	TESTP96	TESTP57	TESTP56	VSS	TESTP55	U
VCC	VSS	VCC			VCC	VCC	VCC_HI	VCC_HI	VCC_HI	TESP74	TESTP79	VSS	TESTP60	TESTP59	VCC	T
VSS	VCC	VSS			VCC	VCC	VCC_HI	VCC_HI	VCC_HI	VCC_HI	VCC_HI	TESTP63	TESTP61	VSS	TESTP58	R
VCC	VSS	VCC			VCC	VCC	VCC	VCC_HI	VCC_HI	VCC_HI	VCC_HI	VSS	VSS	TESTP31	TESTP62	P
					VCC	VCC	VCC	VCC	VCC	VCC_HI	VCC_HI	VCC	VCC	VSS	TESTP30	N
					VCC	VCC	VCC	VCC	VCC	VCC	VCC_HI	VCC_AGP	VCC	VCC	VSS	M
VTT	VTT	VTT	VTT	VSS	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	L
VSS	VSS	VSS	VSS	VTT	TESTP0	TESTP1	TESTP2	TESTP3	VSS	VCC	VCC	VCC	VCC	VCC	VCC	K
VSS	HD59#	VSS	HTRDY#	VSS	HA13#	VSS	HA10#	VSS	HA14#	VCC	VCC	VCC	VCC	VCC	VCC	J
HD61#	VSS	BREQ0#	VSS	HA6#	VSS	HA12#	VSS	HA16#	VSS	VTT	VTT	VSS	VCC	VCC	VCC	H
HD56#	HD58#	HREQ4#	HREQ2#	HA4#	RS2#	RS1#	HADSTB0#	HA11#	GCLKIN	VTT	VTT	VTT	VCC	VCC	VCC	G
VSS	HDVREF0	VSS	HREQ1#	VSS	HA7#	VSS	HA9#	VSS	HA15#	VSS	VTT	VTT	VSS	VCC	VCC	F
HD57#	HD63#	HD60#	HA3#	HREQ3#	HREQ0#	HA5#	HA8#	HCLKP	HCLKN	VTT	VTT	VTT	VTT	VSS	VCC	E
HADSTB1#	VSS	HA29#	VSS	RS0#	VSS	DEFER#	VSS	HA26#	VSS	VTT	VTT	VTT	VTT	VCC33V	VSS	D
BSEL1	BSEL0	BPRI#	HA22#	HA30#	HLOCK#	PROCHOT#	HA21#	HA27#	HA31#	VTT	VTT	VTT	VTT	VCCA_FSB	NC	C
VSS	HA28#	VSS	BNR#	VSS	HA20#	VSS	DBSY#	VSS	HIT#	VSS	VTT	VTT	VTT	NC		B
VTT	HA25#	HA23#	HA24#	HDRCOMP	DRDY#	VTT	ADS#	HITM#	HDVREF1	HDSWING	RSVD	VTT	NC			A
16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

Table 26. MCH Ballout by Signal Name

Signal Name	Ball #
ADS#	A9
BNR#	B13
BPRI#	C14
BREQ0#	H14
BSEL0	C15
BSEL1	C16
CI_RCOMP	AF2
CI_SWING	AE3
CI_VREF	AG1
CI0	AG9
CI1	AK9
CI2	AL9
CI3	AH9
CI4	AF7
CI5	AF6
CI6	AG6
CI7	AH5
CI8	AH7
CI9	AE7
CI10	AH8
CISTRF	AK7
CISTRS	AJ8
CPURST#	H18
TESTP30	N1
TESTP31	P2
DBSY#	B9
DEFER#	D10
DINV0#	B31
DINV1#	F25
DINV2#	C20
DINV3#	J17
DRDY#	A11
EXTTS#	AF14
TESTP32	AK1
TESTP33	AK2
TESTP34	AJ1
TESTP35	AK3
TESTP36	AJ3
TESTP37	AJ4
TESTP38	AH2
TESTP39	AH1
TESTP40	AF5
TESTP41	AE4
TESTP42	AE5

Signal Name	Ball #
TESTP43	AD5
TESTP44	AD6
TESTP45	AD8
TESTP46	AC4
TESTP47	AC8
TESTP48	AA4
TESTP49	Y2
TESTP50	Y1
TESTP51	W1
TESTP52	Y3
TESTP53	W4
TESTP54	W3
TESTP55	U1
TESTP56	U3
TESTP57	U4
TESTP58	R1
TESTP59	T2
TESTP60	T3
TESTP61	R3
TESTP62	P1
TESTP63	R4
TESTP64	AF3
TESTP65	V1
TESTP66	AG3
TESTP67	V2
TESTP68	AG4
TESTP69	AC5
TESTP70	AA3
TESTP71	V3
GCLKIN	G7
TESTP72	AB2
TESTP73	AB7
TESTP74	T6
TESTP75	AB6
TESTP76	AB3
TESTP77	V7
TESTP78	AC3
TESTP79	T5
TESTP80	V5
TESTP81	V6
TESTP82	Y7
TESTP83	W7
TESTP84	AA8
TESTP85	Y5

Signal Name	Ball #
TESTP86	AA5
TESTP87	AA7
TESTP88	Y6
TESTP89	W5
TESTP90	U7
TESTP91	U8
TESTP92	W8
TESTP93	AB5
TESTP94	AB1
GVREF	AD2
TESTP95	AC1
TESTP96	U5
HA3#	E13
HA4#	G12
HA5#	E10
HA6#	H12
HA7#	F11
HA8#	E9
HA9#	F9
HA10#	J9
HA11#	G8
HA12#	H10
HA13#	J11
HA14#	J7
HA15#	F7
HA16#	H8
HA17#	A17
HA18#	C17
HA19#	B17
HA20#	B11
HA21#	C9
HA22#	C13
HA23#	A14
HA24#	A13
HA25#	A15
HA26#	D8
HA27#	C8
HA28#	B15
HA29#	D14
HA30#	C12
HA31#	C7
HADSTB0#	G9
HADSTB1#	D16
HCLKN	E7

Table 26. MCH Ballout by Signal Name (Continued)

Signal Name	Ball #	Signal Name	Ball #	Signal Name	Ball #
HCLKP	E8	HD43#	B19	HI8	AL7
HD0#	C29	HD44#	C18	HI9	AN4
HD1#	D28	HD45#	C19	HI10	AM6
HD2#	A28	HD46#	D18	HISTRF	AK6
HD3#	E27	HD47#	A18	HISTRS	AL5
HD4#	E28	HD48#	J19	HIT#	B7
HD5#	C27	HD49#	G20	HITM#	A8
HD6#	C28	HD50#	E20	HLOCK#	C11
HD7#	B29	HD51#	E18	HREQ0#	E11
HD8#	A29	HD52#	E19	HREQ1#	F13
HD9#	B27	HD53#	G18	HREQ2#	G13
HD10#	D26	HD54#	E17	HREQ3#	E12
HD11#	C26	HD55#	F17	HREQ4#	G14
HD12#	B25	HD56#	G16	HTRDY#	J13
HD13#	A27	HD57#	E16	NC	AN31
HD14#	A25	HD58#	G15	NC	AN3
HD15#	C25	HD59#	J15	NC	AM32
HD16#	J21	HD60#	E14	NC	AM2
HD17#	H23	HD61#	H16	NC	AL33
HD18#	H20	HD62#	G17	NC	AL1
HD19#	H24	HD63#	E15	NC	C33
HD20#	G26	HDRCOMP	A12	NC	C1
HD21#	H22	HDSTBN0#	A26	NC	B32
HD22#	G23	HDSTBN1#	E22	NC	B2
HD23#	G25	HDSTBN2#	B23	NC	A31
HD24#	G21	HDSTBN3#	F19	NC	A3
HD25#	E24	HDSTBP0#	E26	PROCHOT#	C10
HD26#	E25	HDSTBP1#	F21	PWROK	AE9
HD27#	G24	HDSTBP2#	D22	RSVD	AG8
HD28#	F23	HDSTBP3#	G19	RSVD	A5
HD29#	G22	HDSWING	A6	RSVD	AC9
HD30#	E23	HDVREF0	F15	RSVD	AM31
HD31#	E21	HDVREF1	A7	RSVD	AL32
HD32#	A23	HI_RCOMP	AD1	RSVD	AN9
HD33#	C23	HI_SWING	AD3	RSVD	AC7
HD34#	C24	HI_VREF	AF1	RS0#	D12
HD35#	A21	HI00	AL4	RS1#	G10
HD36#	D24	HI1	AK5	RS2#	G11
HD37#	C22	HI2	AM4	RSTIN#	AE8
HD38#	C21	HI3	AJ6	SBA_A0	W31
HD39#	A22	HI4	AN6	SBA_A1	AB30
HD40#	D20	HI5	AL8	SBA_B0	V26
HD41#	B21	HI6	AM8	SBA_B1	AB31
HD42#	A19	HI7	AN7	SCAS_A#	T33

Table 26. MCH Ballout by Signal Name (Continued)

Signal Name	Ball #	Signal Name	Ball #	Signal Name	Ball #
SCAS_B#	R25	SDQ_A3	AM16	SDQ_A47	M33
SCKE_A0	AM24	SDQ_A4	AN14	SDQ_A48	L31
SCKE_A1	AL22	SDQ_A5	AK16	SDQ_A49	L32
SCKE_A2	AL23	SDQ_A6	AL16	SDQ_A50	H30
SCKE_A3	AN23	SDQ_A7	AN16	SDQ_A51	G33
SCKE_B0	AE21	SDQ_A8	AL17	SDQ_A52	L33
SCKE_B1	AF21	SDQ_A9	AN17	SDQ_A53	K33
SCKE_B2	AG20	SDQ_A10	AL21	SDQ_A54	H33
SCKE_B3	AH19	SDQ_A11	AM22	SDQ_A55	H31
SCMDCLK_A0	AE31	SDQ_A12	AL18	SDQ_A56	F33
SCMDCLK_A0#	AE32	SDQ_A13	AN19	SDQ_A57	F31
SCMDCLK_A1	AN20	SDQ_A14	AK20	SDQ_A58	D31
SCMDCLK_A1#	AM21	SDQ_A15	AN21	SDQ_A59	E31
SCMDCLK_A2	J32	SDQ_A16	AK24	SDQ_A60	G32
SCMDCLK_A2#	J33	SDQ_A17	AN25	SDQ_A61	G31
SCMDCLK_A3	AG32	SDQ_A18	AK26	SDQ_A62	E33
SCMDCLK_A3#	AG33	SDQ_A19	AM28	SDQ_A63	E32
SCMDCLK_A4	AM19	SDQ_A20	AN24	SDQ_B0	AG14
SCMDCLK_A4#	AL19	SDQ_A21	AM25	SDQ_B1	AL13
SCMDCLK_A5	K30	SDQ_A22	AN27	SDQ_B2	AK14
SCMDCLK_A5#	K31	SDQ_A23	AL28	SDQ_B3	AJ15
SCMDCLK_B0	AE29	SDQ_A24	AN29	SDQ_B4	AJ13
SCMDCLK_B0#	AD29	SDQ_A25	AL29	SDQ_B5	AM13
SCMDCLK_B1	AG18	SDQ_A26	AJ31	SDQ_B6	AJ14
SCMDCLK_B1#	AF18	SDQ_A27	AH30	SDQ_B7	AH15
SCMDCLK_B2	M30	SDQ_A28	AJ27	SDQ_B8	AG15
SCMDCLK_B2#	M29	SDQ_A29	AJ28	SDQ_B9	AG16
SCMDCLK_B3	AD27	SDQ_A30	AK31	SDQ_B10	AK18
SCMDCLK_B3#	AC27	SDQ_A31	AH31	SDQ_B11	AE19
SCMDCLK_B4	AG17	SDQ_A32	AA28	SDQ_B12	AJ16
SCMDCLK_B4#	AH17	SDQ_A33	AA33	SDQ_B13	AE17
SCMDCLK_B5	M26	SDQ_A34	Y33	SDQ_B14	AG19
SCMDCLK_B5#	M27	SDQ_A35	W32	SDQ_B15	AJ18
SCS_A0#	T31	SDQ_A36	AA31	SDQ_B16	AG21
SCS_A1#	P32	SDQ_A37	AA32	SDQ_B17	AH21
SCS_A2#	T30	SDQ_A38	Y31	SDQ_B18	AH23
SCS_A3#	R33	SDQ_A39	W33	SDQ_B19	AG24
SCS_B0#	P26	SDQ_A40	V33	SDQ_B20	AJ20
SCS_B1#	T29	SDQ_A41	U32	SDQ_B21	AF22
SCS_B2#	T27	SDQ_A42	P31	SDQ_B22	AJ23
SCS_B3#	R27	SDQ_A43	N31	SDQ_B23	AJ24
SDQ_A0	AL15	SDQ_A44	V30	SDQ_B24	AJ25
SDQ_A1	AM15	SDQ_A45	U33	SDQ_B25	AJ26
SDQ_A2	AJ17	SDQ_A46	M31	SDQ_B26	AG27

Table 26. MCH Ballout by Signal Name (Continued)

Signal Name	Ball #	Signal Name	Ball #	Signal Name	Ball #
SDQ_B27	AD26	SDQS_A7	F30	SMAA_B4	AF27
SDQ_B28	AF25	SDQS_A8	AF33	SMAA_B5	AF24
SDQ_B29	AE25	SDQS_B0	AL14	SMAA_B6	AG25
SDQ_B30	AE26	SDQS_B1	AF16	SMAA_B7	AG23
SDQ_B31	AG28	SDQS_B2	AJ21	SMAA_B8	AE23
SDQ_B32	Y26	SDQS_B3	AG26	SMAA_B9	AJ22
SDQ_B33	AA29	SDQS_B4	W25	SMAA_B10	AA25
SDQ_B34	W27	SDQS_B5	R28	SMAA_B11	AG22
SDQ_B35	V27	SDQS_B6	L29	SMAA_B12	AL20
SDQ_B36	Y27	SDQS_B7	K26	SMVREF_A	C32
SDQ_B37	Y29	SDQS_B8	AC28	SMVREF_B	AN12
SDQ_B38	W28	SECC_A0	AG30	SMXRCOMP	AG13
SDQ_B39	W29	SECC_A1	AF31	SMXRCOMPVOH	AN13
SDQ_B40	U27	SECC_A2	AE33	SMXRCOMPVOL	AH13
SDQ_B41	T26	SECC_A3	AC33	SMYRCOMP	AD31
SDQ_B42	P27	SECC_A4	AJ33	SMYRCOMPVOH	N32
SDQ_B43	N25	SECC_A5	AH33	SMYRCOMPVOL	N33
SDQ_B44	V29	SECC_A6	AC31	SRAS_A#	V31
SDQ_B45	U25	SECC_A7	AB33	SRAS_B#	U28
SDQ_B46	R29	SECC_B0	AE28	SWE_A#	U31
SDQ_B47	P30	SECC_B1	AF29	SWE_B#	U29
SDQ_B48	N29	SECC_B2	AB27	TESTP0	K11
SDQ_B49	N27	SECC_B3	AA27	TESTP1	K10
SDQ_B50	K29	SECC_B4	AE27	TESTP2	K9
SDQ_B51	L25	SECC_B5	AC25	TESTP3	K8
SDQ_B52	P29	SECC_B6	AD32	TESTP4	AK13
SDQ_B53	N28	SECC_B7	AB29	TESTP5	AH16
SDQ_B54	L28	SMAA_A0	AC29	TESTP6	AH26
SDQ_B55	L27	SMAA_A1	AH32	TESTP7	AF28
SDQ_B56	K27	SMAA_A2	AG31	TESTP8	W30
SDQ_B57	H29	SMAA_A3	AJ29	TESTP9	U30
SDQ_B58	G29	SMAA_A4	AK30	TESTP10	R26
SDQ_B59	H27	SMAA_A5	AN28	TESTP11	N26
SDQ_B60	J29	SMAA_A6	AK28	TESTP12	AE30
SDQ_B61	J28	SMAA_A7	AM27	TESTP13	AK29
SDQ_B62	J27	SMAA_A8	AL27	TESTP14	AM30
SDQ_B63	G28	SMAA_A9	AL26	TESTP15	AK22
SDQS_A0	AN15	SMAA_A10	AD30	TESTP16	AF19
SDQS_A1	AJ19	SMAA_A11	AN26	TESTP17	AE13
SDQS_A2	AL25	SMAA_A12	AL24	TESTP18	AM18
SDQS_A3	AL30	SMAA_B0	AB26	TESTP19	AH20
SDQS_A4	AA30	SMAA_B1	AH29	TESTP20	AH24
SDQS_A5	R31	SMAA_B2	AG29	TESTP21	AB32
SDQS_A6	J31	SMAA_B3	AH27	TESTP22	T32

Table 26. MCH Ballout by Signal Name (Continued)

Signal Name	Ball #
TESTP23	L30
TESTP24	E29
TESTP25	AC26
TESTP26	AK32
TESTP27	AH25
TESTP28	AK23
TESTP29	AK21
VCC	Y20
VCC	Y18
VCC	Y16
VCC	Y14
VCC	W19
VCC	W17
VCC	W15
VCC	V20
VCC	V18
VCC	V16
VCC	V14
VCC	V11
VCC	U19
VCC	U17
VCC	U15
VCC	U11
VCC	T20
VCC	T18
VCC	T16
VCC	T14
VCC	T11
VCC	T10
VCC	R19
VCC	R17
VCC	R15
VCC	R11
VCC	R10
VCC	P20
VCC	P18
VCC	P16
VCC	P14
VCC	P11
VCC	P10
VCC	P9
VCC	N11
VCC	N10
VCC	N9

Signal Name	Ball #
VCC	N8
VCC	N7
VCC	M11
VCC	M10
VCC	M9
VCC	M8
VCC	M7
VCC	M6
VCC	L11
VCC	L10
VCC	L9
VCC	L8
VCC	L7
VCC	L6
VCC	L5
VCC	K6
VCC	K5
VCC	J6
VCC	J5
VCC	AE1
VCC	AA1
VCC	T1
VCC	N4
VCC	N3
VCC	M4
VCC	M3
VCC	M2
VCC	L4
VCC	L3
VCC	L2
VCC	L1
VCC	K4
VCC	K3
VCC	K2
VCC	K1
VCC	J4
VCC	J3
VCC	J2
VCC	J1
VCC	H3
VCC	H2
VCC	H1
VCC	G3
VCC	G2

Signal Name	Ball #
VCC	G1
VCC	F1
VCC_DDR	AN30
VCC_DDR	AN22
VCC_DDR	AN18
VCC_DDR	AN11
VCC_DDR	AN10
VCC_DDR	AM12
VCC_DDR	AM11
VCC_DDR	AM10
VCC_DDR	AL12
VCC_DDR	AL11
VCC_DDR	AL10
VCC_DDR	AK12
VCC_DDR	AK11
VCC_DDR	AK10
VCC_DDR	AJ12
VCC_DDR	AJ11
VCC_DDR	AJ10
VCC_DDR	AH12
VCC_DDR	AH11
VCC_DDR	AH10
VCC_DDR	AG12
VCC_DDR	AG11
VCC_DDR	AG10
VCC_DDR	AF12
VCC_DDR	AF11
VCC_DDR	AF10
VCC_DDR	AE15
VCC_DDR	AE12
VCC_DDR	AE11
VCC_DDR	AE10
VCC_DDR	AD33
VCC_DDR	AD24
VCC_DDR	AD22
VCC_DDR	AD20
VCC_DDR	AD18
VCC_DDR	AD16
VCC_DDR	AD14
VCC_DDR	AD12
VCC_DDR	AD11
VCC_DDR	AD10
VCC_DDR	AC21
VCC_DDR	AC19

Table 26. MCH Ballout by Signal Name (Continued)

Signal Name	Ball #	Signal Name	Ball #	Signal Name	Ball #
VCC_DDR	AC17	VCC_HI	AN5	VSS	W26
VCC_DDR	AC15	VCC_HI	AA10	VSS	W24
VCC_DDR	AC13	VCC33 V	D2	VSS	W20
VCC_DDR	AC12	VCC	F2	VSS	W18
VCC_DDR	AC11	VCC	E1	VSS	W16
VCC_DDR	AC10	VCCA_DDR	AK33	VSS	W14
VCC_DDR	AB24	VCCA_DDR	AC23	VSS	W6
VCC_DDR	AA23	VCCA_DDR	AC22	VSS	W2
VCC_DDR	Y24	VCCA_DDR	AB23	VSS	K14
VCC_DDR	W23	VCCA_FSB	C2	VSS	K13
VCC_DDR	V24	VCCA_FSB	A30	VSS	K7
VCC_DDR	U23	VSS	AM29	VSS	J30
VCC_DDR	T24	VSS	AM26	VSS	J26
VCC_DDR	R23	VSS	AM23	VSS	J25
VCC_DDR	P33	VSS	AM20	VSS	J24
VCC_DDR	P24	VSS	AM17	VSS	J23
VCC_DDR	N23	VSS	AM14	VSS	J22
VCC_DDR	D33	VSS	AM9	VSS	J20
VCC_HI	Y11	VSS	AM7	VSS	J18
VCC_HI	Y10	VSS	AC6	VSS	J16
VCC_HI	Y9	VSS	AC2	VSS	J14
VCC_HI	W11	VSS	AB28	VSS	J12
VCC_HI	W10	VSS	AB25	VSS	J10
VCC_HI	W9	VSS	AB11	VSS	J8
VCC_HI	V10	VSS	AB10	VSS	H32
VCC_HI	V9	VSS	AB9	VSS	H28
VCC_HI	U10	VSS	AB8	VSS	H26
VCC_HI	U9	VSS	AB4	VSS	H25
VCC_HI	T9	VSS	AA26	VSS	H21
VCC_HI	T8	VSS	AA24	VSS	H19
VCC_HI	T7	VSS	AA11	VSS	H17
VCC_HI	R9	VSS	AA9	VSS	H15
VCC_HI	R8	VSS	AA6	VSS	H13
VCC_HI	R7	VSS	AA2	VSS	H11
VCC_HI	R6	VSS	Y32	VSS	H9
VCC_HI	R5	VSS	Y30	VSS	H7
VCC_HI	P8	VSS	Y28	VSS	H4
VCC_HI	P7	VSS	Y25	VSS	G30
VCC_HI	P6	VSS	Y23	VSS	G27
VCC_HI	P5	VSS	Y19	VSS	F32
VCC_HI	N6	VSS	Y17	VSS	F29
VCC_HI	N5	VSS	Y15	VSS	AM5
VCC_HI	M5	VSS	Y8	VSS	AM3
VCC_HI	AN8	VSS	Y4	VSS	AL31

Table 26. MCH Ballout by Signal Name (Continued)

Signal Name	Ball #	Signal Name	Ball #	Signal Name	Ball #
VSS	AL6	VSS	U14	VSS	D15
VSS	AL3	VSS	U6	VSS	D13
VSS	AL2	VSS	U2	VSS	D11
VSS	AK27	VSS	T28	VSS	D9
VSS	AK25	VSS	T25	VSS	D7
VSS	AK19	VSS	T23	VSS	D1
VSS	AK17	VSS	T19	VSS	C31
VSS	AK15	VSS	T17	VSS	C30
VSS	AK8	VSS	T15	VSS	AF20
VSS	AK4	VSS	T4	VSS	AF17
VSS	AJ32	VSS	R32	VSS	AF15
VSS	AJ30	VSS	R30	VSS	AF13
VSS	AJ9	VSS	R24	VSS	AF9
VSS	AJ7	VSS	R20	VSS	AF8
VSS	AJ5	VSS	R18	VSS	AF4
VSS	AJ2	VSS	R16	VSS	AE24
VSS	AH28	VSS	R14	VSS	AE22
VSS	AH22	VSS	R2	VSS	AE20
VSS	AH18	VSS	P28	VSS	AE18
VSS	AH14	VSS	F28	VSS	AE16
VSS	AH6	VSS	F27	VSS	AE14
VSS	AH4	VSS	F26	VSS	AE6
VSS	AH3	VSS	F24	VSS	AE2
VSS	AG7	VSS	F22	VSS	AD28
VSS	AG5	VSS	F20	VSS	AD25
VSS	AG2	VSS	F18	VSS	AD23
VSS	AF32	VSS	F16	VSS	AD21
VSS	AF30	VSS	F14	VSS	AD19
VSS	AF26	VSS	F12	VSS	AD17
VSS	AF23	VSS	F10	VSS	AD15
VSS	V32	VSS	F8	VSS	AD13
VSS	V28	VSS	F6	VSS	AD9
VSS	V25	VSS	F3	VSS	AD7
VSS	V23	VSS	E30	VSS	AD4
VSS	V19	VSS	E2	VSS	AC32
VSS	V17	VSS	D32	VSS	AC30
VSS	V15	VSS	D30	VSS	AC24
VSS	V8	VSS	D29	VSS	AC20
VSS	V4	VSS	D27	VSS	AC18
VSS	U26	VSS	D25	VSS	AC16
VSS	U24	VSS	D23	VSS	AC14
VSS	U20	VSS	D21	VSS	P25
VSS	U18	VSS	D19	VSS	P23
VSS	U16	VSS	D17	VSS	P19

Table 26. MCH Ballout by Signal Name (Continued)

Signal Name	Ball #
VSS	P17
VSS	P15
VSS	P4
VSS	P3
VSS	N30
VSS	N24
VSS	N2
VSS	M32
VSS	M28
VSS	M25
VSS	M24
VSS	M23
VSS	M1
VSS	L26
VSS	L24
VSS	L23
VSS	L12
VSS	K32
VSS	K28
VSS	K25
VSS	K24
VSS	K23
VSS	K22
VSS	K21
VSS	K20
VSS	K19
VSS	K18
VSS	K17
VSS	K16
VSS	K15
VSS	B30
VSS	B28
VSS	B26
VSS	B24
VSS	B22
VSS	B20
VSS	B18
VSS	B16
VSS	B14
VSS	B12
VSS	B10
VSS	B8
VSS	B6
VTT	E4

Signal Name	Ball #
VTT	E3
VTT	D6
VTT	D5
VTT	D4
VTT	D3
VTT	C6
VTT	C5
VTT	C4
VTT	C3
VTT	B5
VTT	B4
VTT	L22
VTT	L21
VTT	L20
VTT	L19
VTT	L18
VTT	L17
VTT	L16
VTT	L15
VTT	L14
VTT	L13
VTT	K12
VTT	H6
VTT	H5
VTT	G6
VTT	G5
VTT	G4
VTT	F5
VTT	F4
VTT	E6
VTT	E5
VTT	B3
VTT	A24
VTT	A20
VTT	A16
VTT	A10
VTT	A4

7.2 Package Information

The MCH is in a 42.5 mm x 42.5 mm FC-BGA package with 1005 solder balls and 1 mm ball pitch. Figure 14 through Figure 16 show the package dimensions.

Figure 14. Intel® E7210 MCH Package Dimensions (Top View)

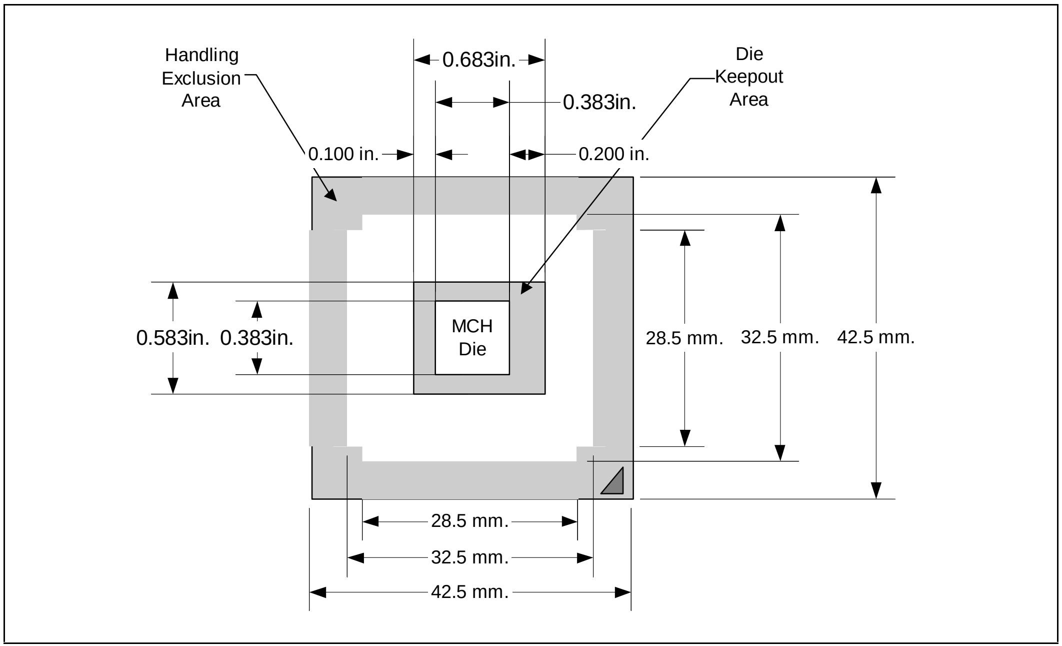
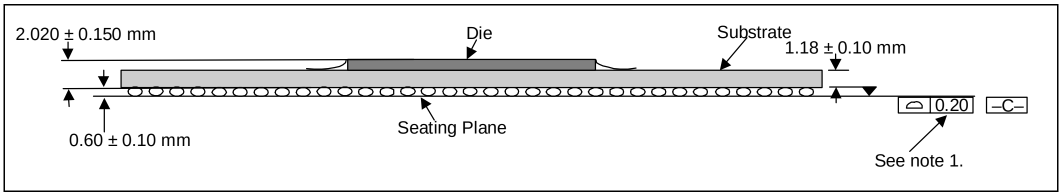
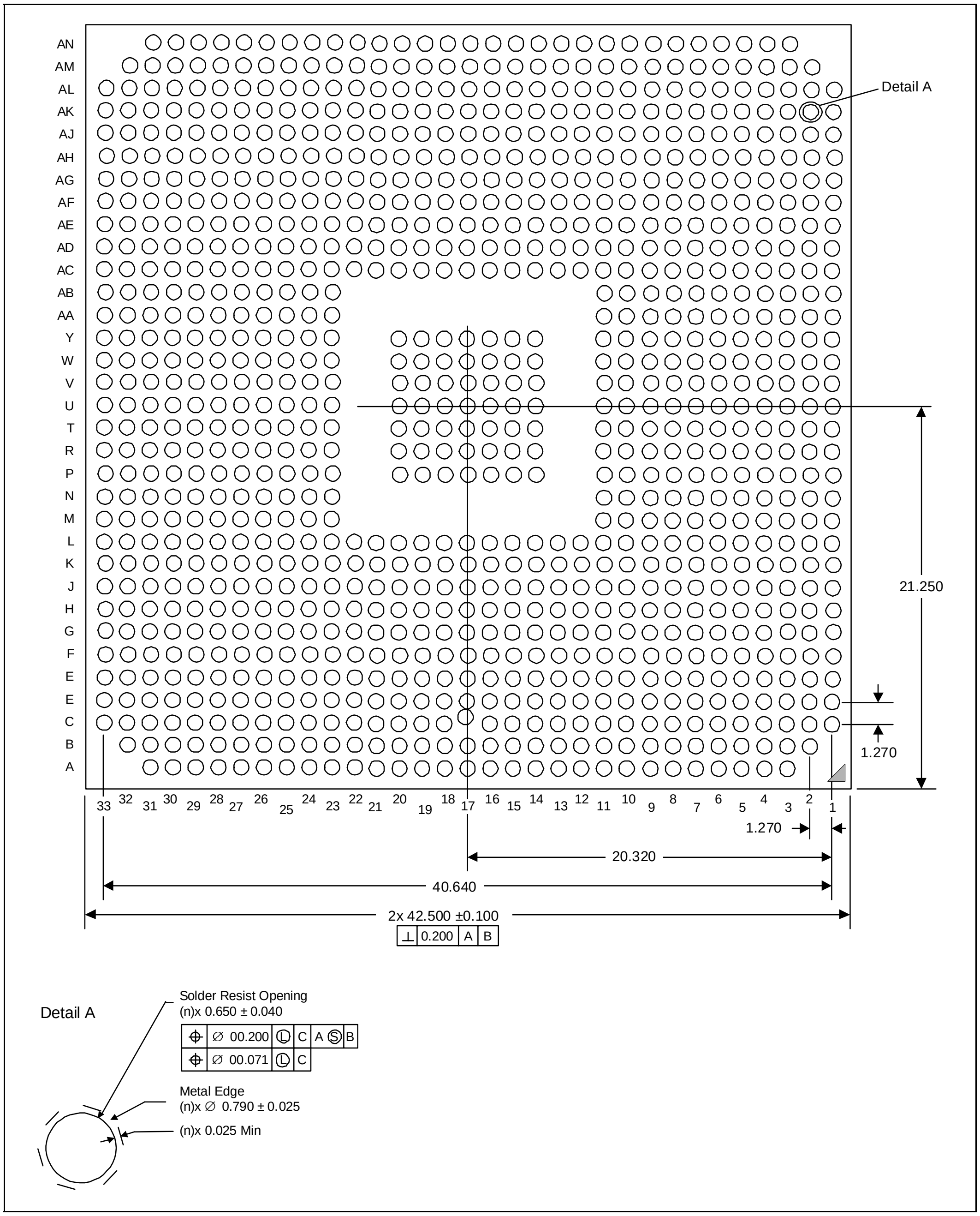


Figure 15. Intel® E7210 MCH Package Dimensions (Side View)



NOTES:
1. Primary datum —C— and seating plane are defined by the spherical crowns of the solder balls.
2. All dimensions and tolerances conform to ANSI Y14.5M–1994.

Figure 16. Intel® E7210 MCH Package Dimensions (Bottom View)



NOTES:

1. All dimensions are in millimeters.
2. All dimensions and tolerances conform to ANSI Y14.5M–1994.

§

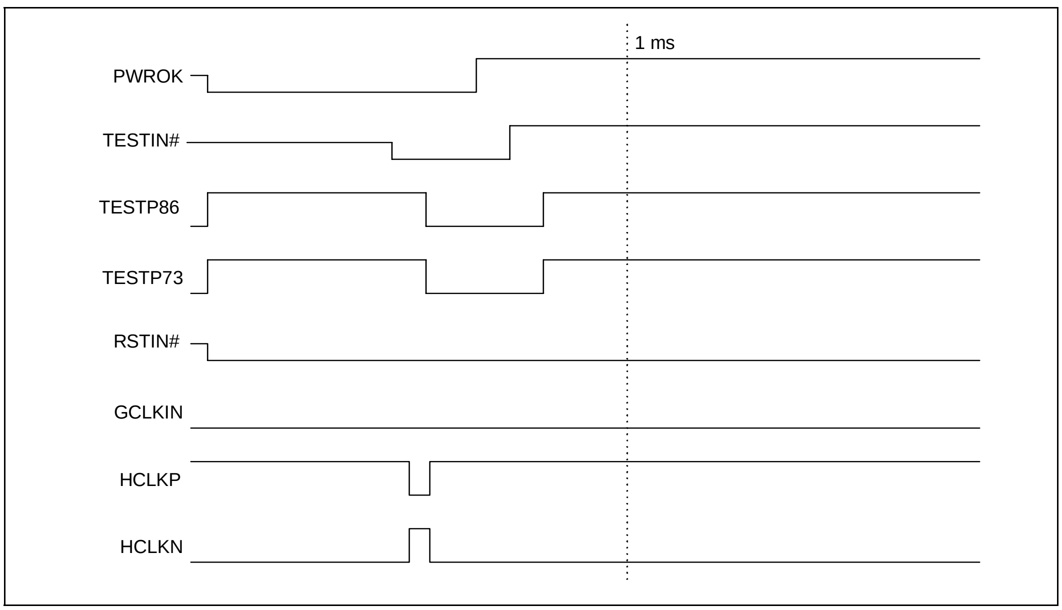
Testability 8

In the MCH, testability for Automated Test Equipment (ATE) board level testing has been implemented as an XOR chain. An XOR-tree is a chain of XOR gates, each with one input pin connected to it.

8.1 XOR Test Mode Initialization

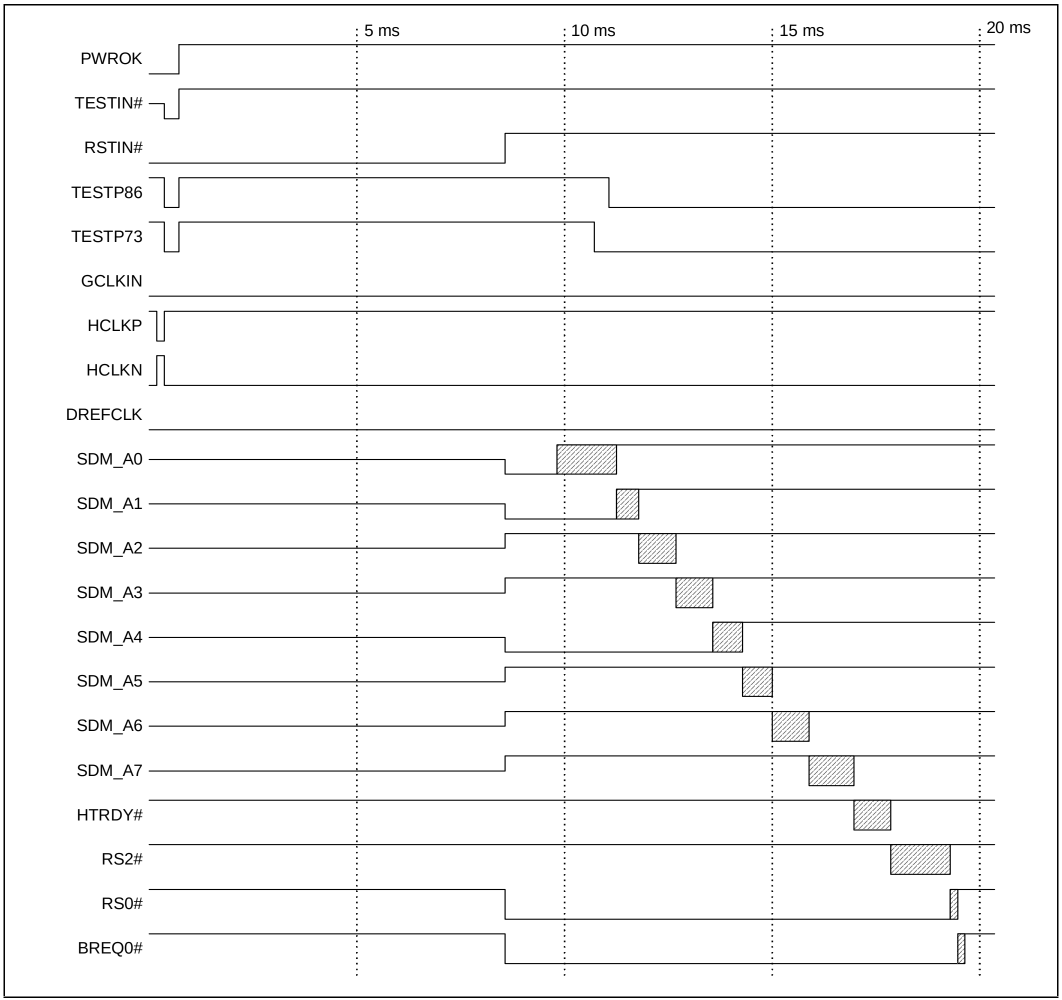
XOR test mode can be entered by driving TESTP86, TESTP87, TESTIN#, PWROK low, and RSTIN# low, then driving PWROK high, then RSTIN# high. XOR test mode via TESTIN# (pin AC9) does not require a clock. But toggling of HCLKP and HCLKN as shown in Figure 17 is required for deterministic XOR operation. This applies to AGP 2.0 mode. If the part is in AGP 3.0 mode, TESTP86, TESTP86, and TESTP69 must be driven high.

Figure 17. XOR Toggling of HCLKP and HCLKN



Pin testing will not start until RSTIN# is de-asserted. Figure 18 shows chains are tested sequentially. Note that for the MCH, sequential testing is not required. All chains can be tested in parallel for test time reduction.

Figure 18. XOR Testing Chains Tested Sequentially



8.1.1 XOR Chain Definition

The MCH has 12 XOR chains. The XOR chain outputs are driven out on the output pins shown in Table 26. During fullwidth testing, XOR chain outputs will be visible on both pins. (For example, xor_out0 is visible on SDM_A0 and SDM_B0.) During channel shared mode on the tester, outputs are visible on their respective channels. (For example, in channel A mode, xor_out0 is visible on SDM_A0 and the same is visible on SDM_B0 in channel B mode.)

Table 26. XOR Chain Outputs

XOR Chain	DDR Output Pin Channel A	DDR Output Pin Channel B
xor_out0	TESTP17	TESTP4
xor_out1	TESTP18	TESTP5
xor_out2	TESTP19	TESTP6
xor_out3	TESTP20	TESTP7
xor_out4	TESTP21	TESTP8
xor_out5	TESTP22	TESTP9
xor_out6	TESTP23	TESTP10
xor_out7	TESTP24	TESTP11
xor_out8	HTRDY#	BPRI#
xor_out9	RS2#	DEFER#
xor_out10	RS0#	RS1#
xor_out11	BREQ0#	CPURST#

Table 27 through Table 39 shows the XOR chain pin mappings and their monitors for the MCH.

Note: Notes for Table 27 through Table 39.

1. All XOR chains can be run in parallel.
2. The channel A and channel B output pins for each chain show the same output.

Table 27. XOR Chain 0 (60 Inputs) Output Pins: TESTP17, TESTP4

Signal Name	Ball Number	Signal Name	Ball Number	Signal Name	Ball Number
CI7	AH5	TESTP35	AK3	TESTP90	U7
CI1	AK9	TESTP68	AG4	TESTP75	AB6
CI2	AL9	TESTP64	AF3	TESTP70	AA3
CI8	AH7	TESTP44	AD6	TESTP71	V3
CI9	AE7	TESTP39	AH1	TESTP92	W8
CI0	AG9	TESTP93	AB5	TESTP30	N1
CISTRF	AK7	TESTP43	AD5	TESTP79	T5
CISTRS	AJ8	TESTP42	AE5	TESTP82	Y7
CI6	AG6	TESTP41	AE4	TESTP88	Y6
CI3	AH9	TESTP47	AC8	TESTP87	AA7
CI4	AF7	TESTP45	AD8	TESTP80	V5
CI5	AF6	TESTP46	AC4	TESTP85	Y5
CI10	AH8	TESTP94	AB1	TESTP83	W7
TESTP33	AK2	TESTP76	AB3	TESTP84	AA8
TESTP37	AJ4	TESTP69	AC5	TESTP81	V6
TESTP32	AK1	TESTP73	AB7	TESTP86	AA5
TESTP38	AH2	TESTP31	P2	TESTP2	K9
TESTP34	AJ1	TESTP72	AB2	TESTP3	K8
TESTP36	AJ3	TESTP77	V7	TESTP0	K11
TESTP40	AF5	TESTP96	U5	RSVD	AC7
Output Pins					
TESTP17	AE13				
TESTP4	AK13				

Table 28. XOR Chain 1 (33 Inputs) Output Pins: TESTP18, TESTP5

Signal Name	Ball Number	Signal Name	Ball Number	Signal Name	Ball Number
HI7	AN7	HI8	AL7	TESTP55	U1
HI4	AN6	HI9	AN4	TESTP57	U4
HI3	AJ6	TESTP91	U8	TESTP59	T2
HI5	AL8	TESTP52	Y3	TESTP56	U3
HISTRF	AK6	TESTP48	AA4	TESTP53	W4
HI10	AM6	TESTP49	Y2	TESTP60	T3
HISTRS	AL5	TESTP51	W1	TESTP62	P1
HI2	AM4	TESTP50	Y1	TESTP63	R4
HI0	AL4	TESTP65	V1	TESTP61	R3
HI6	AM8	TESTP54	W3	TESTP74	T6
HI1	AK5	TESTP58	R1	EXTTS#	AF14
Output Pins					
TESTP18	AM18				
TESTP5	AH16				

Table 29. XOR Chain 2 (44 Inputs) Output Pins: TESTP19, TESTP6

Signal Name	Ball Number	Signal Name	Ball Number	Signal Name	Ball Number
TESTP66	AG3	HD19#	H24	HDSTBN0#	A26
TESTP89	W5	HD27#	G24	HD6#	C28
HD29#	G22	HD24#	G21	HD9#	B27
HD25#	E24	HD21#	H22	HD12#	B25
HD26#	E25	HD28#	F23	HD3#	E27
HD31#	E21	HD16#	J21	HD2#	A28
HD22#	G23	HD18#	H20	HD0#	C29
HD17#	H23	DINV0#	B31	HD4#	E28
HD30#	E23	HD8#	A29	HD5#	C27
HD20#	G26	HD11#	C26	HD7#	B29
DINV1#	F25	HD14#	A25	HD1#	D28
HD23#	G25	HD10#	D26	PROCHOT#	C10
HDSTBP1#	F21	HD15#	C25	HITM#	A8
HDSTBN1#	E22	HD13#	A27	BSEL0	C15
		HDSTBP0#	E26	HLOCK#	C11
Output Pins					
TESTP19	AH20				
TESTP6	AH26				

Table 30. XOR Chain 3 (41 Inputs) Output Pins: TESTP20, TESTP7

Signal Name	Ball Number	Signal Name	Ball Number	Signal Name	Ball Number
BNR#	B13	HA12#	H10	HA19#	B17
BSEL1	C16	HA9#	F9	HA18#	C17
HIT#	B7			HA22#	C13
DRDY#	A11	HA4#	G12	HA24#	A13
DBSY#	B9	HA10#	J9	HA23#	A14
ADS#	A9	HA15#	F7	HADSTB1#	D16
HREQ4#	G14	HA8#	E9	HA17#	A17
HA16#	H8	HA13#	J11	HA25#	A15
HREQ3#	E12	HA6#	H12	HA20#	B11
HREQ0#	E11	HA5#	E10	HA30#	C12
HA3#	E13	HA11#	G8	HA21#	C9
HREQ1#	F13	HREQ2#	G13	HA27#	C8
HA7#	F11	HA31#	C7	HA29#	D14
HA14#	J7	HA26#	D8	HA28#	B15
Output Pins					
TESTP20	AH24				
TESTP7	AF28				

Table 31. XOR Chain 4 (40 Inputs) Output Pins: TESTP21, TESTP8

Signal Name	Ball Number	Signal Name	Ball Number	Signal Name	Ball Number
HD45#	C19	HD43#	B19	HD57#	E16
HD46#	D18	HD33#	C23	HDSTBP3#	G19
HD40#	D20	HD41#	B21	HDSTBN3#	F19
HD47#	A18	HD35#	A21	HD51#	E18
HD39#	A22	HD32#	A23	HD49#	G20
HD36#	D24	HD37#	C22	HD55#	F17
HD44#	C18	HD58#	G15	HD54#	E17
HD42#	A19	HD56#	G16	HD53#	G18
DINV2#	C20	HD62#	G17	HD50#	E20
HDSTBP2#	D22	HD61#	H16	HD48#	J19
HDSTBN2#	B23	HD63#	E15	HD52#	E19
HD34#	C24	HD59#	J15	DINV3#	J17
HD38#	C21	HD60#	E14	TESTP65	V1
Output Pins				TESTP1	K10
TESTP21	AB32				
TESTP8	W30				

Table 32. XOR Chain 5 (44 Inputs) Output Pins: TESTP22, TESTP9

Signal Name	Ball Number	Signal Name	Ball Number	Signal Name	Ball Number
SDQ_A58	D31	SDQ_A53	K33	SDQ_A41	U32
SDQ_A59	E31	SDQ_A48	L31	SDQ_A44	V30
SDQ_A62	E33	SDQ_A52	L33	SDQS_A4	AA30
SDQ_A63	E32	SDQ_A49	L32	SDQ_A35	W32
SDQS_A7	F30	SCMDCLK_A5#	K31	SDQ_A38	Y31
SDQ_A61	G31	SCMDCLK_A5	K30	SDQ_A39	W33
SDQ_A57	F31	SCMDCLK_A2#	J33	SDQ_A34	Y33
SDQ_A56	F33	SCMDCLK_A2	J32	SDQ_A33	AA33
SDQ_A60	G32	SDQS_A5	R31	SDQ_A37	AA32
SDQ_A51	G33	SDQ_A42	P31	SDQ_A36	AA31
SDQ_A50	H30	SDQ_A46	M31	SDQ_A32	AA28
SDQ_A55	H31	SDQ_A47	M33	SCMDCLK_A0	AE31
SDQS_A6	J31	SDQ_A43	N31	SCMDCLK_A0#	AE32
SDQ_A54	H33	SDQ_A40	V33	SCMDCLK_A3#	AG33
		SDQ_A45	U33	SCMDCLK_A3	AG32
Output Pins					
TESTP22	T32				
TESTP9	U30				

Table 33. XOR Chain 6 (40 Inputs) Output Pins: TESTP23, TESTP10

Signal Name	Ball Number	Signal Name	Ball Number	Signal Name	Ball Number
SDQ_A30	AK31	SDQ_A19	AM28	SDQ_A8	AL17
SDQS_A3	AL30	SDQ_A23	AL28	SDQ_A6	AL16
SDQ_A27	AH30	SDQ_A22	AN27	SDQ_A2	AJ17
SDQ_A31	AH31	SDQ_A16	AK24	SDQ_A3	AM16
SDQ_A29	AJ28	SDQ_A20	AN24	SDQS_A0	AN15
SDQ_A26	AJ31	SDQ_A10	AL21	SDQ_A5	AK16
SDQ_A25	AL29	SDQ_A15	AN21	SDQ_A7	AN16
SDQ_A24	AN29	SDQ_A14	AK20	SDQ_A4	AN14
SDQ_A28	AJ27	SDQS_A1	AJ19	SCMDCLK_A1	AN20
SDQS_A2	AL25	SDQ_A11	AM22	SCMDCLK_A1#	AM21
SDQ_A21	AM25	SDQ_A13	AN19	SDQ_A1	AM15
SDQ_A17	AN25	SDQ_A9	AN17	SCMDCLK_A4#	AL19
SDQ_A18	AK26	SDQ_A12	AL18	SCMDCLK_A4	AM19
				SDQ_A0	AL15
Output Pins					
TESTP23	L30				
TESTP10	R26				

Table 34. XOR Chain 7 (45 Inputs) Output Pins: TESTP24, TESTP11

Signal Name	Ball Number	Signal Name	Ball Number	Signal Name	Ball Number
HADSTB1#	D16	SDQS_B6	L29	SDQ_B41	T26
SDQ_B57	H29	SDQ_B48	N29	SDQS_B5	R28
SDQ_B61	J28	SDQ_B49	N27	SDQ_B37	Y29
SDQ_B58	G29	SDQ_B52	P29	SDQ_B36	Y27
SDQ_B63	G28	SCMDCLK_B5	M26	SDQ_B35	V27
SDQ_B60	J29	SCMDCLK_B5#	M27	SDQ_B32	Y26
SDQS_B7	K26	SCMDCLK_B2#	M29	SDQ_B34	W27
SDQ_B62	J27	SCMDCLK_B2	M30	SDQ_B38	W28
SDQ_B59	H27	SDQ_B43	N25	SDQ_B33	AA29
SDQ_B56	K27	SDQ_B46	R29	SDQ_B39	W29
SDQ_B51	L25	SDQ_B42	P27	SDQS_B4	W25
SDQ_B54	L28	SDQ_B47	P30	SCMDCLK_B0	AE29
SDQ_B55	L27	SDQ_B45	U25	SCMDCLK_B0#	AD29
SDQ_B53	N28	SDQ_B40	U27	SCMDCLK_B3	AD27
SDQ_B50	K29	SDQ_B44	V29	SCMDCLK_B3#	AC27
Output Pins					
TESTP24	E29				
TESTP11	N26				

Table 35. XOR Chain 8 (40 Inputs) Output Pins: TESTP8, TESTP8

Signal Name	Ball Number	Signal Name	Ball Number	Signal Name	Ball Number
SDQ_B30	AE26	SDQ_B21	AF22	SDQ_B8	AG15
SDQ_B26	AG27	SDQ_B17	AH21	SCMDCLK_B4#	AH17
SDQ_B29	AE25	SDQS_B2	AJ21	SCMDCLK_B4	AG17
SDQ_B27	AD26	SDQ_B16	AG21	SCMDCLK_B1#	AF18
SDQ_B31	AG28	SDQ_B20	AJ20	SCMDCLK_B1	AG18
SDQ_B25	AJ26	SDQ_B10	AK18	SDQ_B1	AL13
SDQS_B3	AG26	SDQ_B14	AG19	SDQ_B3	AJ15
SDQ_B28	AF25	SDQ_B15	AJ18	SDQ_B7	AH14
SDQ_B24	AJ25	SDQ_B11	AE19	SDQ_B2	AK14
SDQ_B23	AJ24	SDQ_B13	AE17	SDQ_B6	AJ14
SDQ_B18	AH23	SDQ_B12	AJ16	SDQ_B5	AM13
SDQ_B19	AG24	SDQ_B9	AG16	SDQ_B0	AG14
SDQ_B22	AJ23	SDQS_B1	AF16	SDQ_B4	AJ13
				SDQS_B0	AL14
Output Pins					
HTRDY#	J13				
BPRI#	C14				

Table 36. XOR Chain 9 (62 Inputs) Output Pins: RSB2, DEFER#

Signal Name	Ball Number	Signal Name	Ball Number	Signal Name	Ball Number
SCAS_A#	T33	SMAA_B0	AB26	SMAA_B7	AG23
SWE_A#	U31	TESTP25	AC26	SMAA_B9	AJ22
SCS_B3#	R27	SMAA_A6	AK28	SMAA_B11	AG22
SBA_B1	AB31	SMAA_B6	AG25	SMAA_B4	AF27
SBA_A1	AB30	TESTP27	AH25	SMAA_B5	AF24
SCS_A1#	P32	TESTP26	AK32	SCKE_A3	AN23
SCS_A2#	T30	SMAA_A3	AJ29	SCKE_A0	AM24
SCS_A3#	T33	SMAA_B3	AH27	SMAA_A11	AN26
SRAS_A#	V31	SMAA_B1	AH29	SMAA_A12	AL24
SBA_A0	W31	TESTP14	AM30	SCKE_A2	AL23
SCS_A0#	T31	SMAA_A4	AK30	SCKE_A1	AL22
SMAA_B2	AG29	TESTP15	AK22	SCKE_B0	AE21
SRAS_B#	U28	TESTP13	AK29	SCKE_B3	AH19
SMAA_B10	AA25	TESTP28	AK23	SCKE_B2	AG20
SBA_B0	V26	TESTP29	AK21	SMAA_B12	AL20
SMAA_A10	AD30	SMAA_A9	AL26	SCKE_B1	AF21
TESTP12	AE30	TESTP16	AF19	SCS_B1#	T29
SMAA_A0	AC29	SMAA_A8	AL27	SCS_B0#	P26
SMAA_A1	AH32	SMAA_A5	AN28	SCS_B2#	T27
SMAA_A2	AG31	SMAA_A7	AM27	SWE_B#	U29

Table 36. XOR Chain 9 (62 Inputs) Output Pins: RSB2, DEFER# (Continued)

Signal Name	Ball Number	Signal Name	Ball Number	Signal Name	Ball Number
		SMAA_B8	AE23	SCAS_B#	T25
Output Pins					
RS2#	G11				
DEFER#	D10				

Table 37. XOR Chain 10 (9 Inputs) Output Pins: RS0#, RS1#

Signal Name	Ball Number	Signal Name	Ball Number	Signal Name	Ball Number
SECC_A5	AH33	SECC_A1	AF31	SDQS_A8	AF33
SECC_A4	AJ33	SECC_A3	AC33	SECC_A7	AB33
SECC_A2	AE33	SECC_A0	AG30	SECC_A6	AC31
Output Pins					
RS0#	D12				
RS1#	G10				

Table 38. XOR Chain 11 (9 Inputs) Output Pins: BREQ0#, CPURST#

Signal Name	Ball Number	Signal Name	Ball Number	Signal Name	Ball Number
SECC_B1	AF29	SECC_B7	AB29	SECC_B3	AA27
SECC_B0	AE28	SECC_B6	AD32	SECC_B5	AC25
SDQS_B8	AC28	SECC_B4	AE27	SECC_B2	AB27
Output Pins					
BREQ0#	H14				
CPURST#	H18				

Table 39. XOR Excluded Pins

Signal Name	Ball Number	Signal Name	Ball Number
BPRI#	C14	TESTP20	AH24
BREQ0#	H14	TESTP21	AB32
CPURST#	H18	TESTP22	T32
DEFER#	D10	TESTP23	L30
GCLKIN	G7	TESTP24	E29
TESTP78	AC3	TESTP4	AK13
GVREF	AD2	TESTP5	AH16
TESTP95	AC1	TESTP6	AH26
HCLKN	E7	TESTP7	AF28
HCLKP	E8	TESTP8	W30
HDRCOMP	A12	TESTP9	U30
HDSWING	A6	TESTP10	R26
HDVREF0	F15	TESTP11	N26

Table 39. XOR Excluded Pins (Continued)

Signal Name	Ball Number	Signal Name	Ball Number
HDVREF1	A7	SMVREF_A	C32
HTRDY#	J13	SMVREF_B	AN12
HI_RCOMP	AD1	SMXRCOMP	AG13
HI_VREF	AF1	SMXRCOMPVOH	AN13
HI_SWING	AD3	SMXRCOMPVOL	AH13
PWROK	AE9	SMYRCOMP	AD31
RS0#	D12	SMYRCOMPVOH	N32
RS1#	G10	SMYRCOMPVOL	N33
RS2#	G11	RESERVED	A5
RSTIN#	AE8	TESTIN#	AC9
TESTP17	AE13	CI_RCOMP	AF2
TESTP18	AM18	CI_VREF	AG1
TESTP19	AH20	CI_SWING	AE3

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